

Compal confidential

Bradford 10AT

NSKAE LA-5381P REV 0.2 Schematics Document

Mobile AMD SIG3/RS880M&RS880MC/SB710
2009-04-10 Rev. 0.2

Security Classification	Compal Secret Data			Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Compal Electronics, Inc. Cover Sheet	
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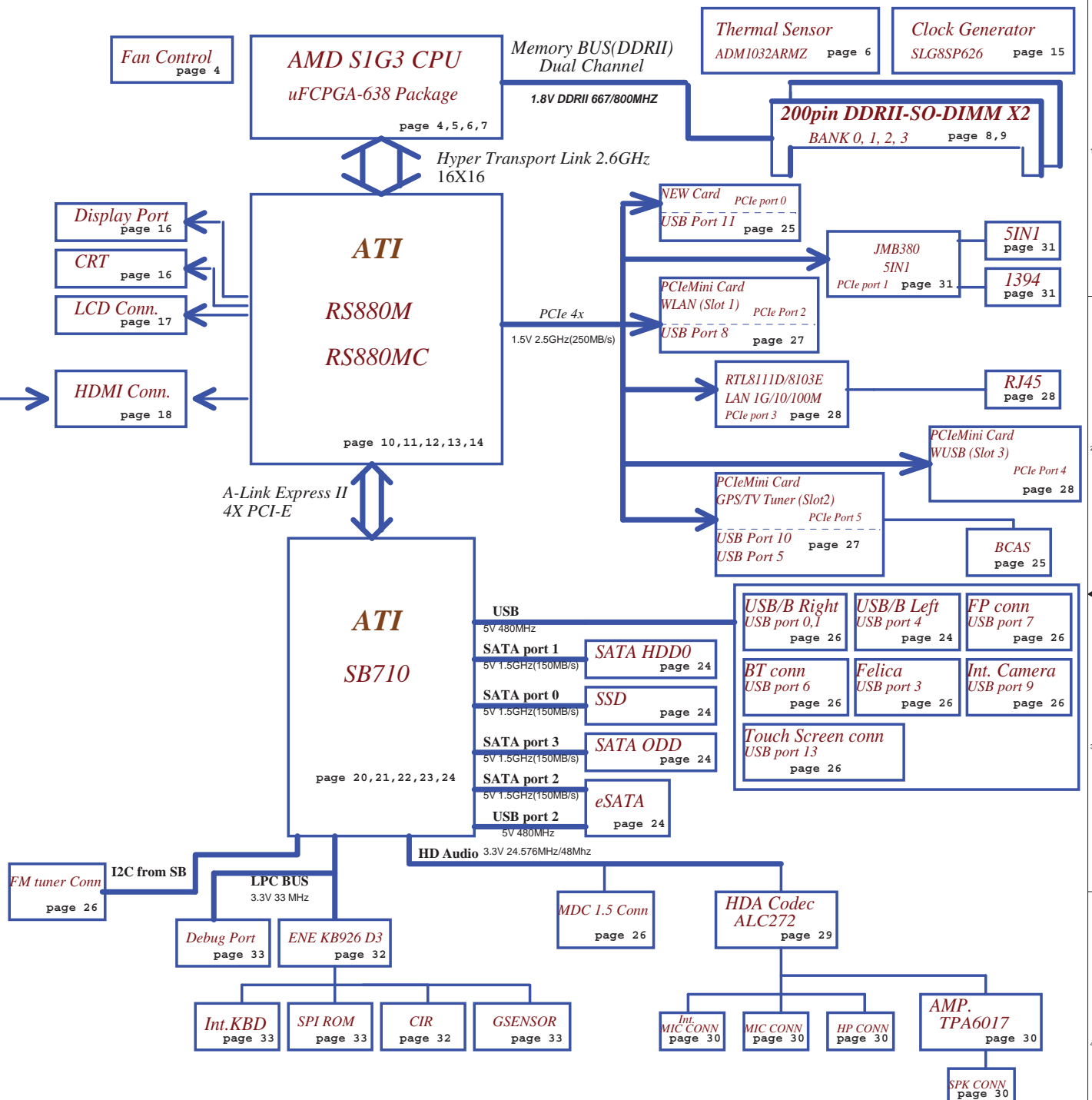
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Model Name : NSKAE

File Name : LA-5381P

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Voltage Rails

O MEANS ON X MEANS OFF

power plane	State	B+	+5VALW	+1.8V	+5VS
		+3VL	+3VALW	+0.9V	+3VS
		+5VL	+1.2VALW		+2.5VS
		+RTCVCC	+3V_LAN		+1.8VS
					+1.5VS
					+1.1VS
					+VGA_CORE
					+1.2V_HT
					+VDDNB
					+CPU_CORE_0
					+CPU_CORE_1
S0		O	O	O	O
S1		O	O	O	O
S3		O	O	O	X
S5 S4/AC		O	O	X	X
S5 S4/ Battery only		O	X	X	X
S5 S4/AC & Battery don't exist		X	X	X	X

Symbol Note :

 : means Digital Ground

 : means Analog Ground

@ : means just reserve , no build

Item	CPU	NB	VGA	SB
	S1G3	RS880MC	NA	SB710
	S1G3	RS880M	NA	SB710

BTO Option Table

Function	HDMI		DIPLAY PORT	Side Port			
description				Memory			
explain	HDMI	CEC	DIPLAY PORT	Side Port	Samsung	Hynix	No Side Port
BTO	HDMI@	HE	DP@	SIDE@	SAMSIDE@	HYNSIDE@	NOSIDE@

Function	MINI PCI-E SLOT			LAN	Felica	BLUETOOTH	CRT	
description								
explain	3G	B-CAS	WIMAX	10/100M	Giga	FELICA	BLUE TOOTH	CRT
BTO	3G@	TV@	WIMAX@	8103EL@	8111DL@	FEL@	BT@	CRT@

Function	G-SENSOR	Modem	FM TUNER	Fingerprint	SSD	CIR
description						
explain	HDD PROTECT	Modem	FM TUNER	Fingerprint		
BTO	GSENSOR@	RJ11@	FM@	FP@	SSD@	CIR@

SB SM Bus1 Address

SB SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	DDR SO-DIMM 0	A0 H	1010 0000 b	+3VALW	WLAN/WIMAX		
+3VS	DDR SO-DIMM 1	A4 H	1010 0100 b				
+3VS	Clock Generator	D2 H	1101 0010 b				
+3VS	New Card						
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VS	FM Tuner				Virtual I2C		

SMBUS Control Table

	SOURCE	New Card	BATT	CEC	THERMAL SENSOR CPU & ADM1032	SODIMM I / II	CLK	3G/TV	LCD	HDMI	Display Port	G-Sensor
SMB_EC_CK1	KB926	X	V	V	X	X	X	X	X	X	X	X
SMB_EC_DA1	KB926	X	V	V	X	X	X	X	X	X	X	X
SMB_EC_CK2	KB926	X	X	X	V	X	X	X	X	X	X	V
SMB_EC_DA2	KB926	X	X	X	V	X	X	X	X	X	X	V
I2C_CLK	RS780M	X	X	X	X	X	X	X	V	X	X	X
I2C_DATA	RS780M	X	X	X	X	X	X	X	V	X	X	X
DDC_CLK0	RS780M	X	X	X	X	X	X	X	X	V	X	X
DDC_DATA0	RS780M	X	X	X	X	X	X	X	X	V	X	X
DDC_CLK1	RS780M	X	X	X	X	X	X	X	X	X	V	X
DDC_DATA1	RS780M	X	X	X	X	X	X	X	X	X	V	X
SCL0	SB700	V	X	X	X	V	V	X	X	X	X	X
SDA0	SB700	V	X	X	X	V	V	X	X	X	X	X
SCL1	SB700	X	X	X	X	X	X	V	X	X	X	X
SDA1	SB700	X	X	X	X	X	X	V	X	X	X	X
SCL2	SB700	X	X	X	X	X	X	X	X	X	X	X
SDA2	SB700	X	X	X	X	X	X	X	X	X	X	X
SCL3	SB700	X	X	X	X	X	X	X	X	X	X	X
SDA3	SB700	X	X	X	X	X	X	X	X	X	X	X

EC SM Bus1 Address

EC SM Bus2 Address

Power	Device	HEX	Address	Power	Device	HEX	Address
+5VL	Smart Battery	16 H	0001 011X b	+3VS	CPU_ADM1032-1	98 H	1001 100X b
+5VL	HDMI-CEC	34 H	0011 010X b	+3VS	VGA_ADM1032-2	9A H	1001 101X b
				+3VS	G-Sensor		
				+3VS	Light Sensor		
Power	Device	HEX	Address	Power	Device	HEX	Address
+3VL	Cap. Sensor		Virtual I2C				

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<10> H_CADIN[0..15] H_CADIN[0..15]

H_CADOP[0..15] H_CADOP[0..15] <10>

H_CADON[0..15] H_CADON[0..15] <10>



H_CADIP0	E3	L0_CADIN_H0	L0_CADOUT_H0	AD1	H_CADOP0
H_CADIN0	E2	L0_CADIN_L0	L0_CADOUT_L0	AC1	H_CADON0
H_CADIP1	F1	L0_CADIN_H1	L0_CADOUT_H1	AC2	H_CADOP1
H_CADIN1	F1	L0_CADIN_L1	L0_CADOUT_L1	AC3	H_CADON1
H_CADIP2	G3	L0_CADIN_H2	L0_CADOUT_H2	AB1	H_CADOP2
H_CADIN2	G2	L0_CADIN_L2	L0_CADOUT_L2	AA1	H_CADON2
H_CADIP3	G1	L0_CADIN_H3	L0_CADOUT_H3	AA2	H_CADOP3
H_CADIN3	G1	L0_CADIN_L3	L0_CADOUT_L3	AA3	H_CADON3
H_CADIP4	H1	L0_CADIN_H4	L0_CADOUT_H4	W2	H_CADOP4
H_CADIN4	K1	L0_CADIN_L4	L0_CADOUT_L4	W3	H_CADON4
H_CADIP5	L3	L0_CADIN_H5	L0_CADOUT_H5	V1	H_CADOP5
H_CADIN5	L2	L0_CADIN_L5	L0_CADOUT_L5	LH1	H_CADON5
H_CADIP6	L2	L0_CADIN_H6	L0_CADOUT_H6	U2	H_CADOP6
H_CADIN6	M1	L0_CADIN_L6	L0_CADOUT_L6	U3	H_CADON6
H_CADIP7	N3	L0_CADIN_H7	L0_CADOUT_H7	T1	H_CADOP7
H_CADIN7	E5	L0_CADIN_L7	L0_CADOUT_L7	R1	H_CADON7
H_CADIP8	N2	L0_CADIN_H8	L0_CADOUT_H8	AD4	H_CADOP8
H_CADIN8	FS	L0_CADIN_L8	L0_CADOUT_L8	AD3	H_CADON8
H_CADIP9	F3	L0_CADIN_H9	L0_CADOUT_H9	AD5	H_CADOP9
H_CADIN9	F4	L0_CADIN_L9	L0_CADOUT_L9	AC5	H_CADON9
H_CADIP10	G5	L0_CADIN_H10	L0_CADOUT_H10	AB4	H_CADOP10
H_CADIN10	H5	L0_CADIN_L10	L0_CADOUT_L10	AB3	H_CADON10
H_CADIP11	H3	L0_CADIN_H11	L0_CADOUT_H11	AB5	H_CADOP11
H_CADIN11	H4	L0_CADIN_L11	L0_CADOUT_L11	AA5	H_CADON11
H_CADIP12	K3	L0_CADIN_H12	L0_CADOUT_H12	YS	H_CADOP12
H_CADIN12	K4	L0_CADIN_L12	L0_CADOUT_L12	W5	H_CADON12
H_CADIP13	L5	L0_CADIN_H13	L0_CADOUT_H13	V4	H_CADOP13
H_CADIN13	M5	L0_CADIN_L13	L0_CADOUT_L13	V3	H_CADON13
H_CADIP14	M3	L0_CADIN_H14	L0_CADOUT_H14	V5	H_CADOP14
H_CADIN14	M4	L0_CADIN_L14	L0_CADOUT_L14	U5	H_CADON14
H_CADIP15	NS	L0_CADIN_H15	L0_CADOUT_H15	T4	H_CADOP15
H_CADIN15	P5	L0_CADIN_L15	L0_CADOUT_L15	T3	H_CADON15

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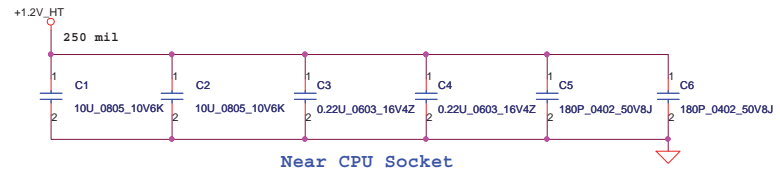
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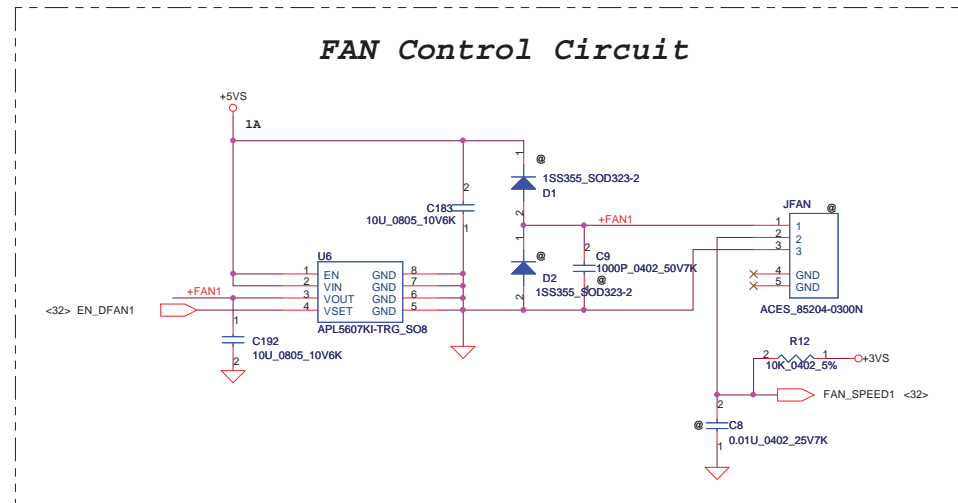
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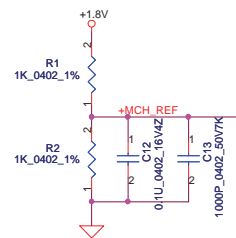


FAN Control Circuit

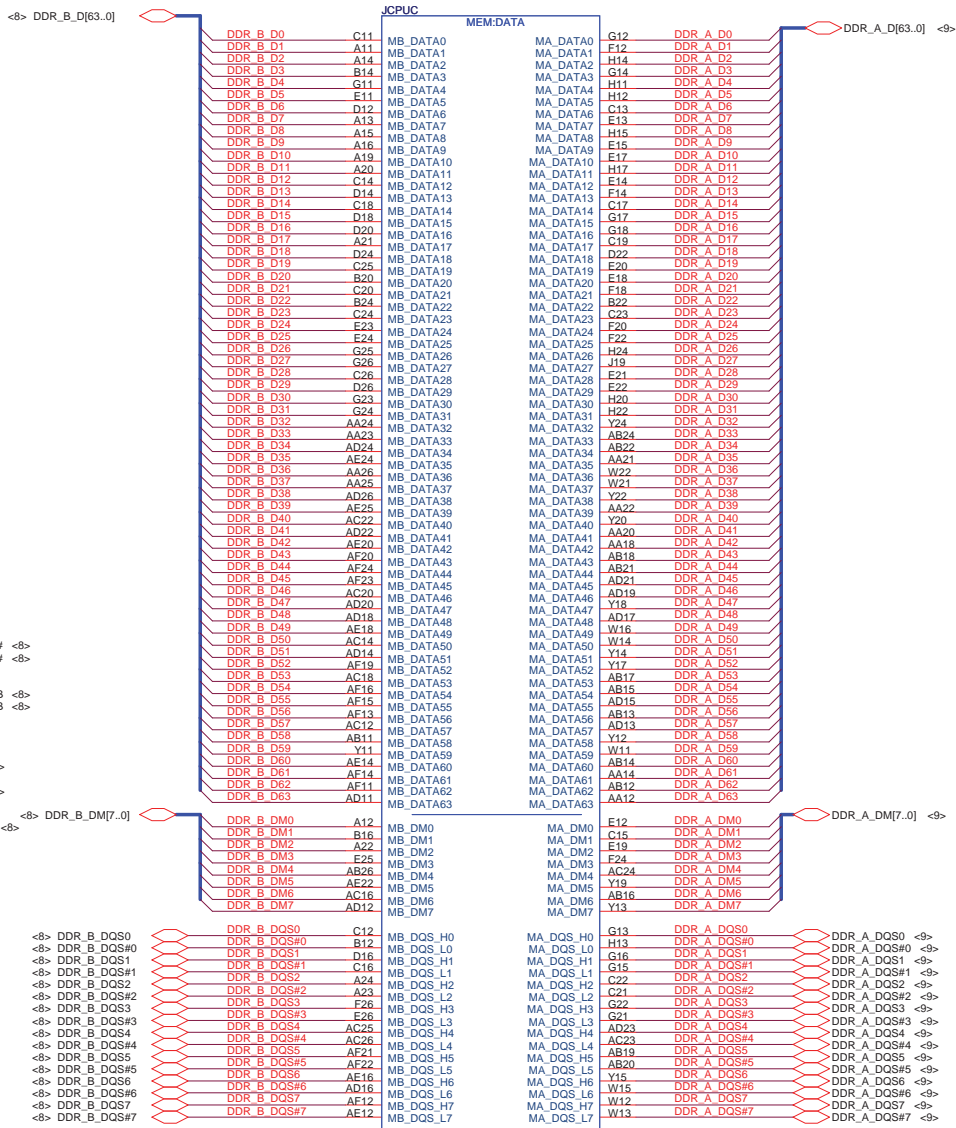
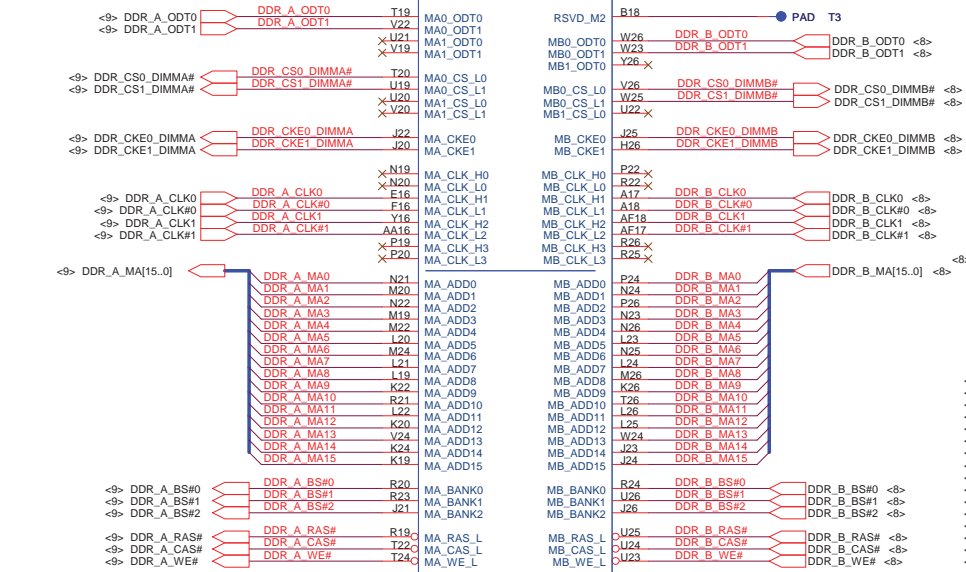
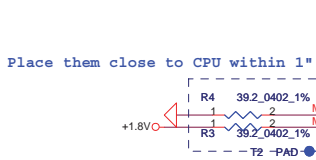
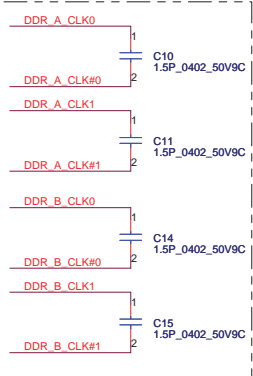


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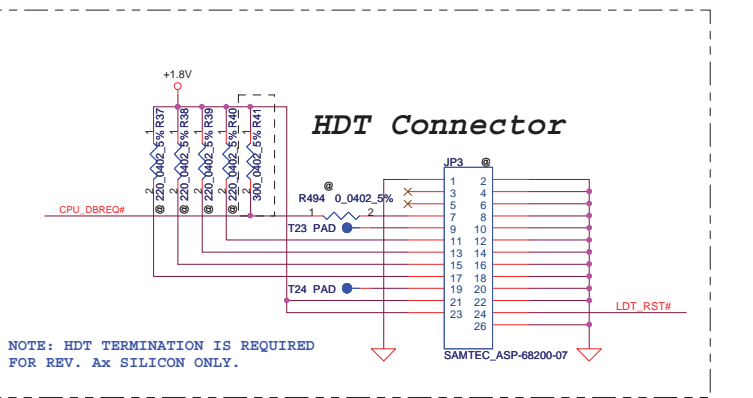
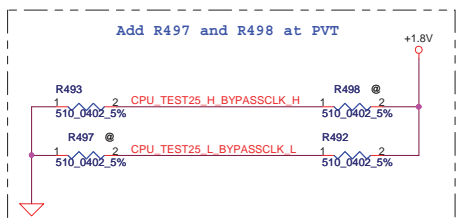
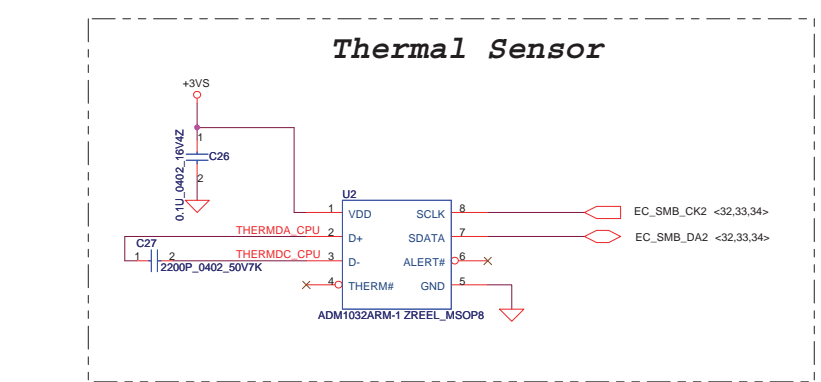
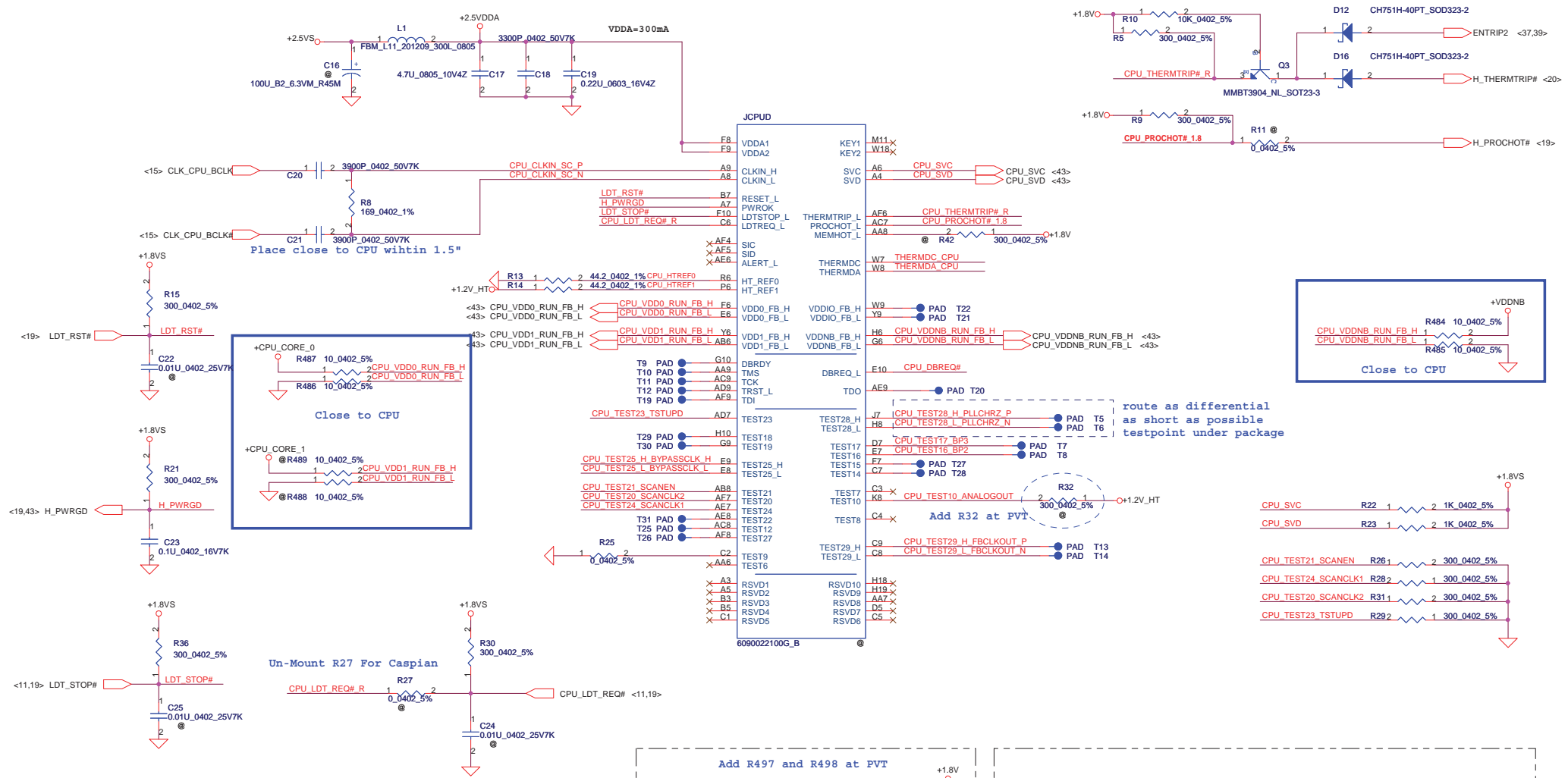
Processor DDR2 Memory Interface



PLACE CLOSE TO PROCESSOR
WITHIN 1.5 INCH

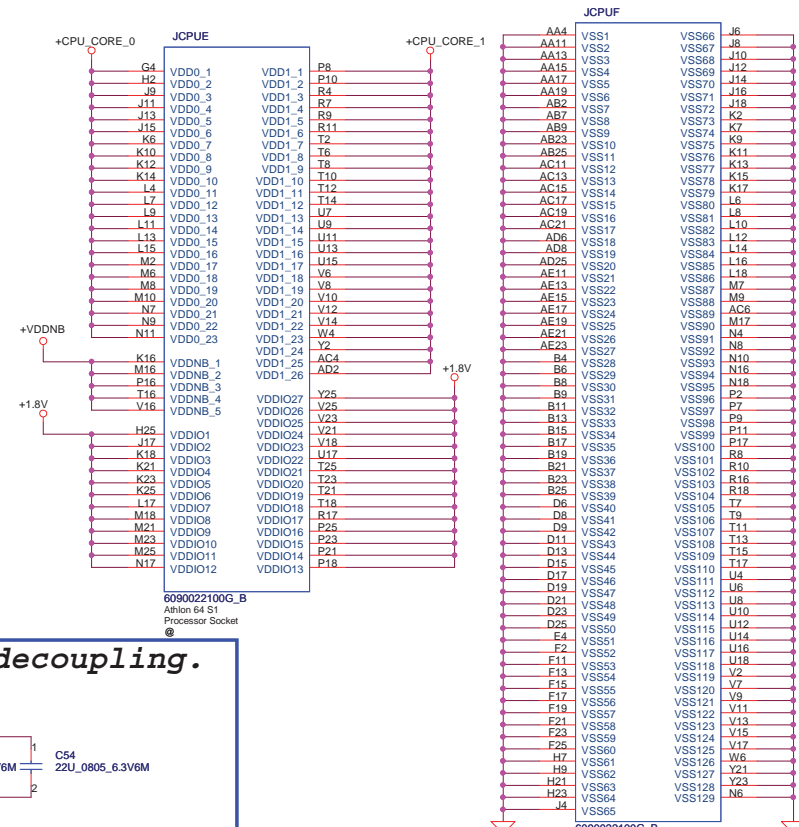
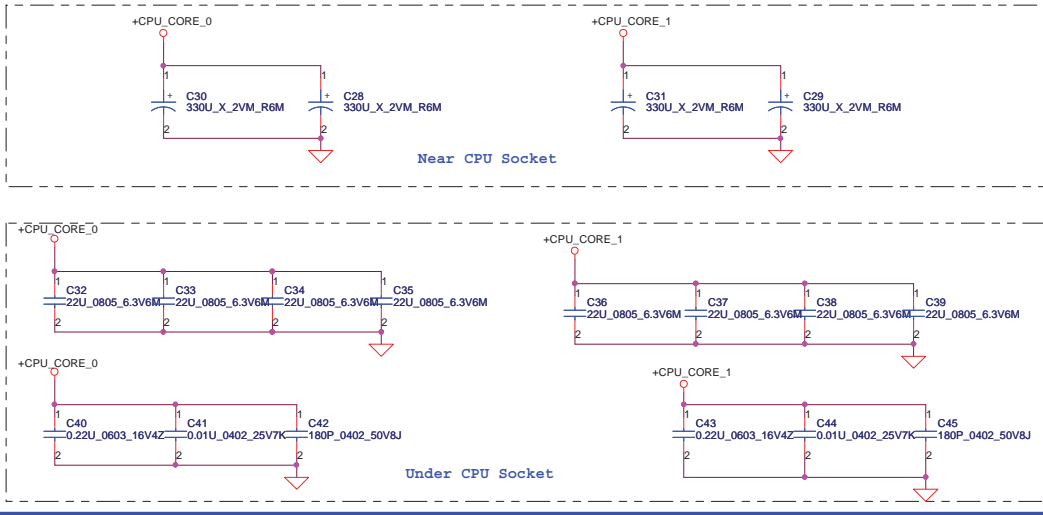


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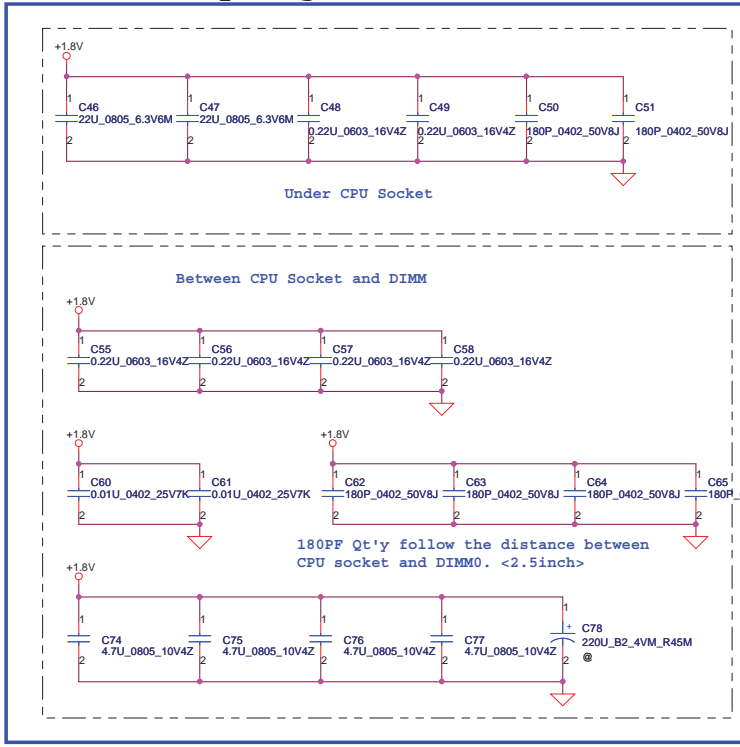


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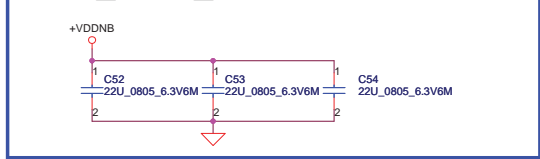
VDD(+CPU_CORE) decoupling.



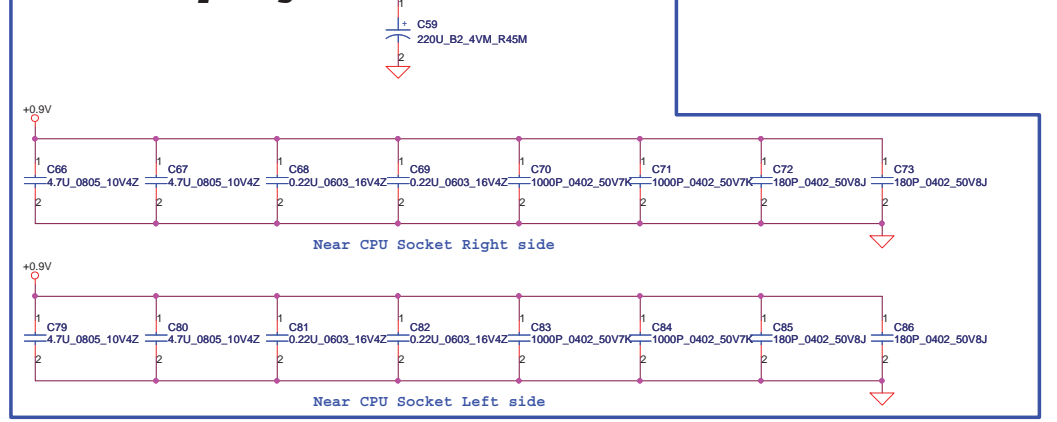
VDDIO decoupling.

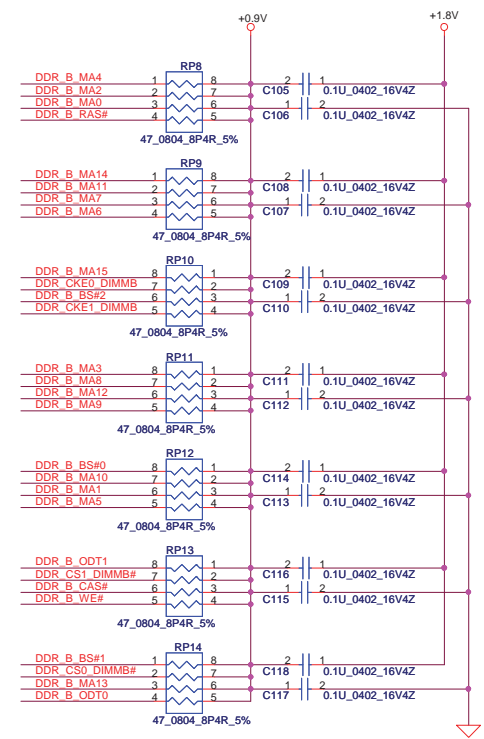
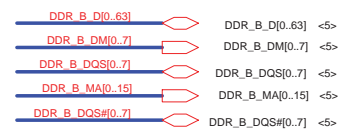
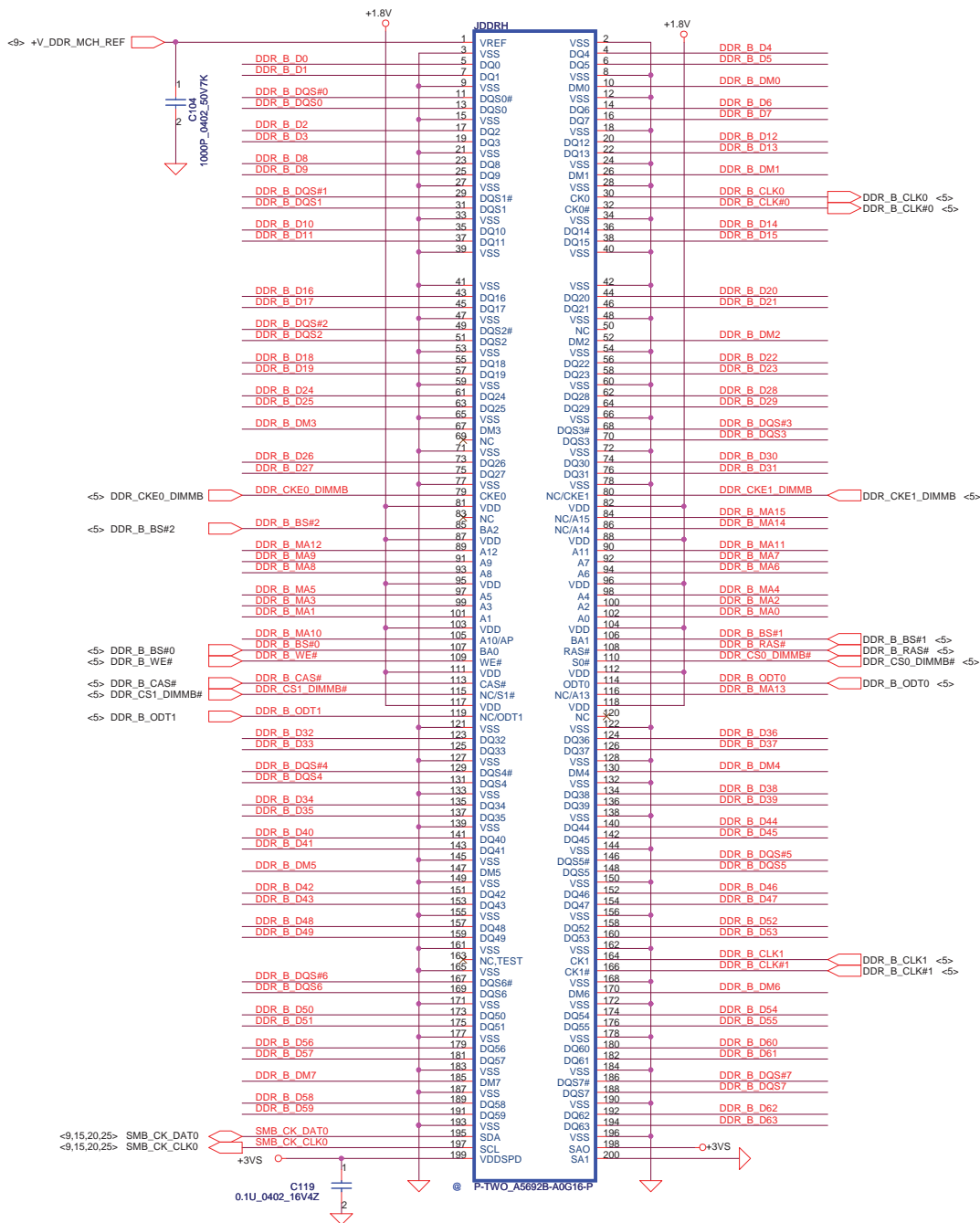


+CPU_CORE NB decoupling.



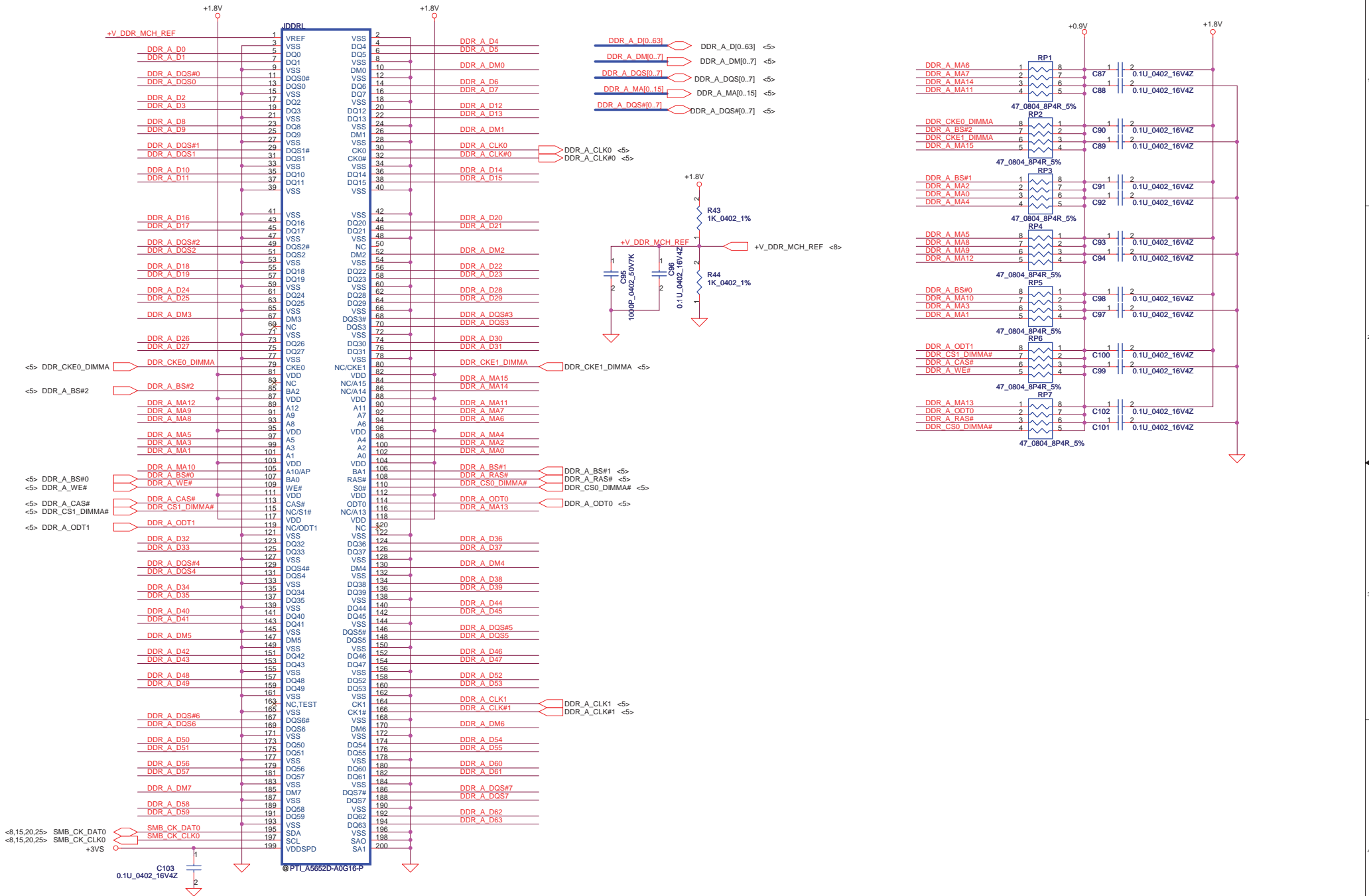
VTT decoupling.





DIMM0 STD H:9.2mm (Bot)

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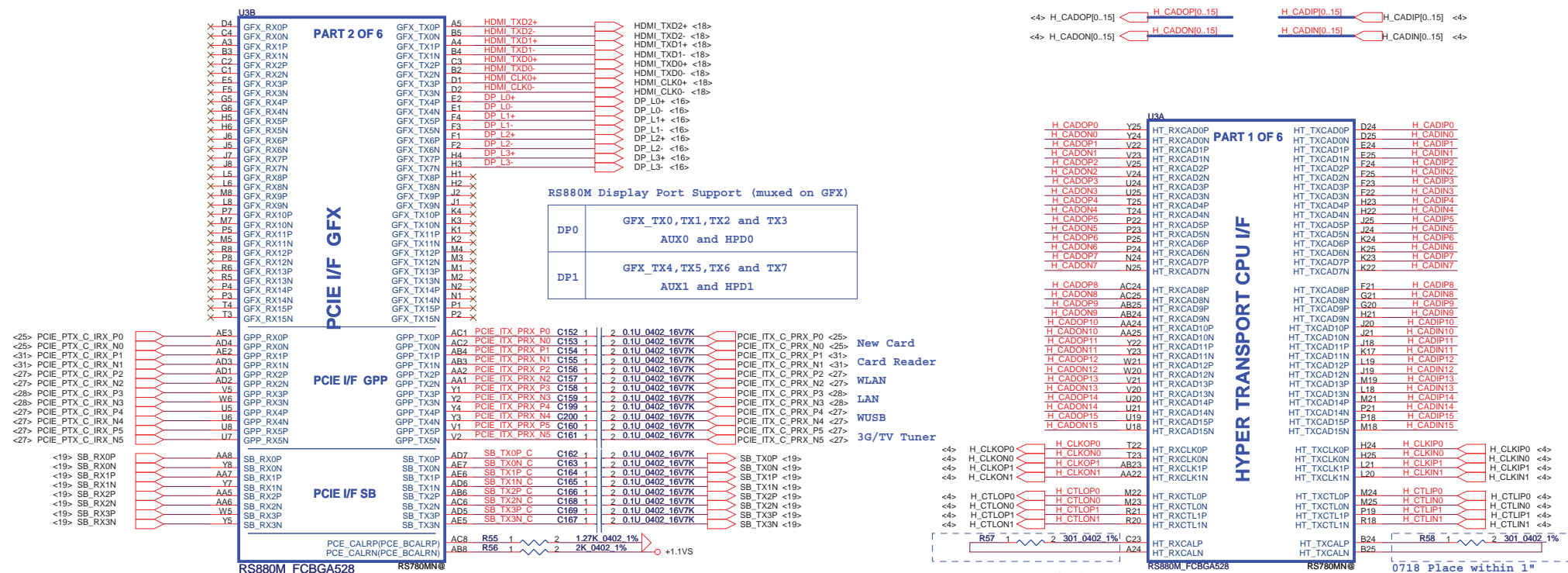
DIMM0 STD H:5.2mm (Bot)

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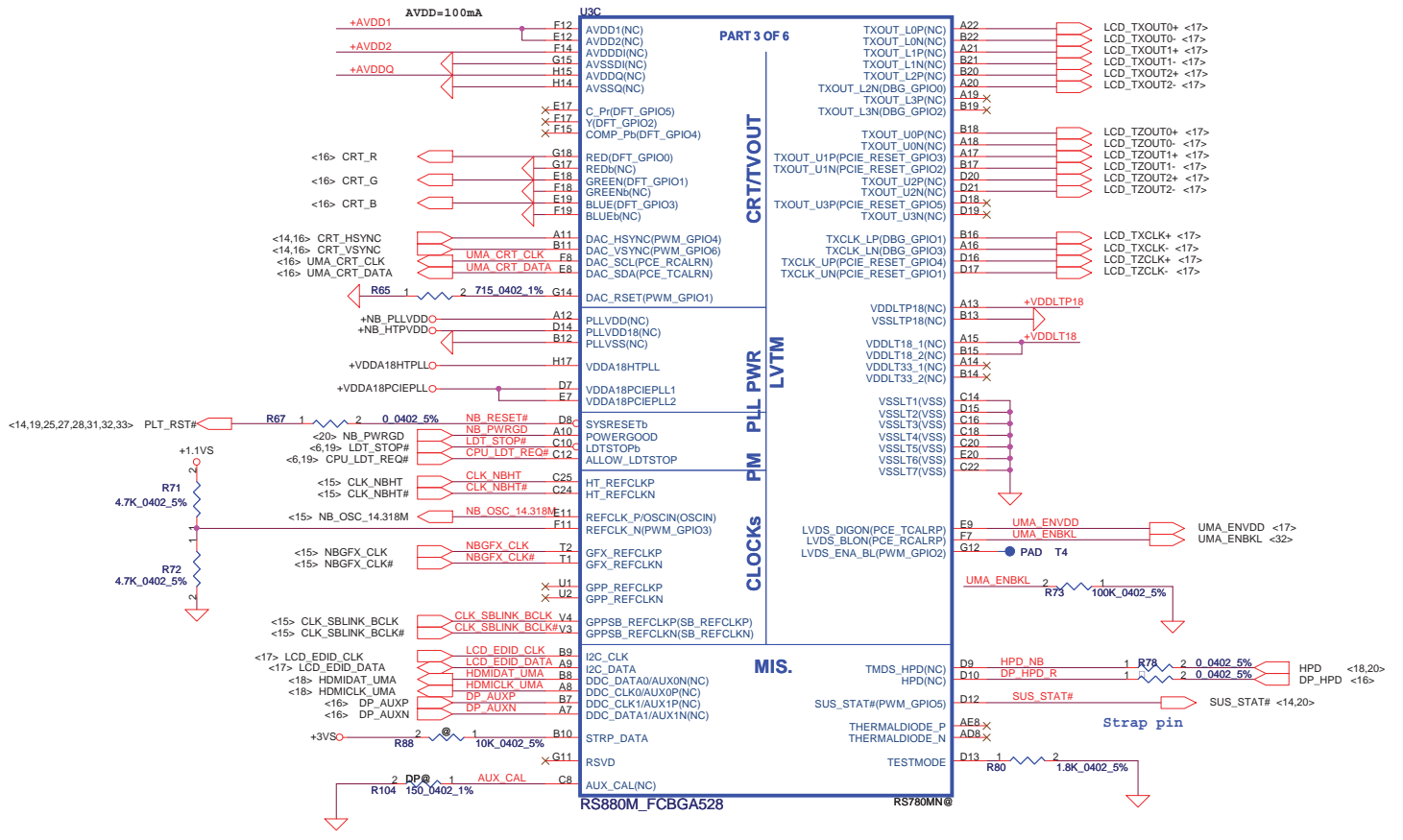
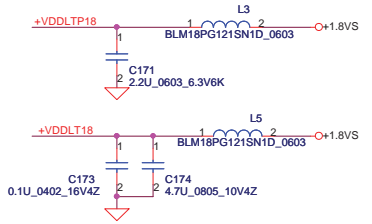
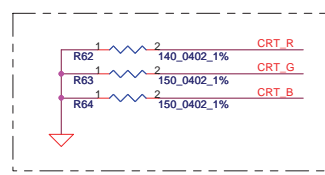
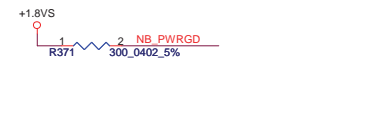
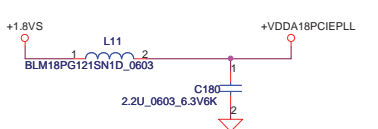
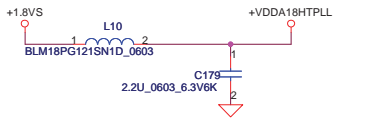
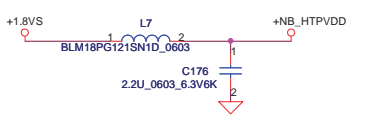
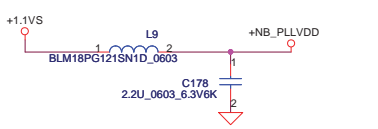
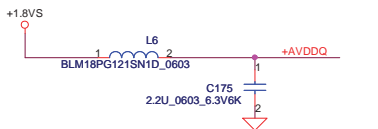
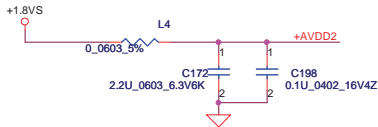
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DDR2 SO-DIMM 1

LA-5381P

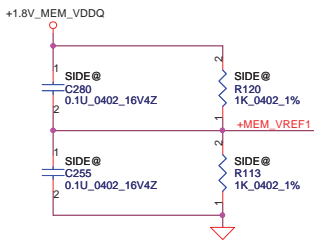
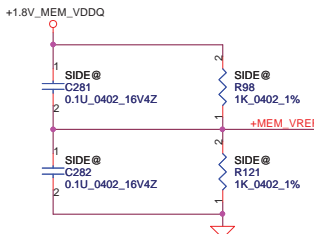
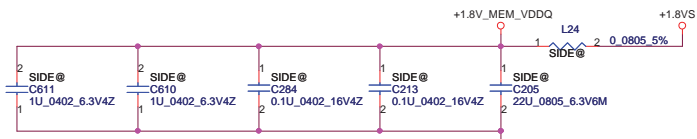


Security Classification	Compal Secret Data		Title		Compal Electronics, Inc.	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Document Number		RS780M&RX781-HT/PCIE
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Date:	Friday, April 10, 2009	Sheet	10	of	46	



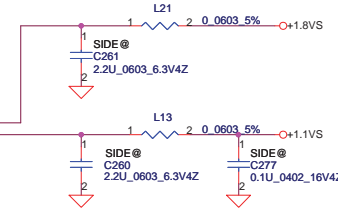
Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	RS780 VEDIO/CLK GEN
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Document Number LA-5381P			Rev 0.2	
Date: Friday, April 10, 2009 Sheet 11 of 46				

220 ohm @ 100MHz,2A

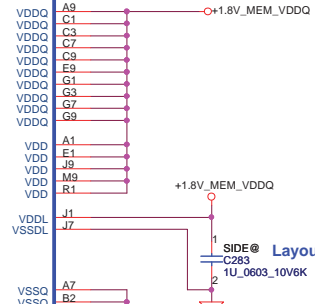
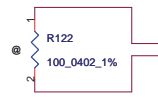


MEM_COMP_P and MEM_COMP_N trace width >=10mils and 10mils spacing from other Signals in X,Y,Z directions

U3D PAR 4 OF 6		
MEM_A0	AB12	MEM_A0(NC)
MEM_A1	AE16	MEM_A1(1NC)
MEM_A2	V11	MEM_A2(1NC)
MEM_A3	AE15	MEM_A3(1NC)
MEM_A4	AA12	MEM_A4(1NC)
MEM_A5	AB16	MEM_A5(1NC)
MEM_A6	AB14	MEM_A6(1NC)
MEM_A7	AD14	MEM_A7(1NC)
MEM_A8	AD13	MEM_A8(1NC)
MEM_A9	AD15	MEM_A9(1NC)
MEM_A10	AC16	MEM_A10(1NC)
MEM_A11	AE13	MEM_A11(1NC)
MEM_A12	AC14	MEM_A12(1NC)
MEM_A13	X-114	MEM_A13(1NC)
MEM_BA0	AD16	MEM_BA0(1NC)
MEM_BA1	AE17	MEM_BA1(1NC)
MEM_BA2	AD17	MEM_BA2(1NC)
MEM_RAS#	W12c	MEM_RASb(1NC)
MEM_CAS#	I12c	MEM_CASb(1NC)
MEM_WE#	AD18c	MEM_WEb(1NC)
MEM_CS#	AB13c	MEM_CSb(1NC)
MEM_CKE	AB18	MEM_CKE(1NC)
MEM_ODT	V14	MEM_ODT(1NC)
MEM_CLKP	V15	MEM_CLKP(1NC)
MEM_CLKN	W14	MEM_CLKN(1NC)
MEM_COMP_P	AE12	MEM_COMP(1NC)
MEM_COMP_N	AD12	MEM_COMP(1NC)
MEM_DQ0	AA18	MEM_DQ0
MEM_DQ1	AA20	MEM_DQ1
MEM_DQ2	AA19	MEM_DQ2
MEM_DQ3	Y19	MEM_DQ3
MEM_DQ4	V17	MEM_DQ4
MEM_DQ5	AA17	MEM_DQ5
MEM_DQ6	AA15	MEM_DQ6
MEM_DQ7	Y15	MEM_DQ7
MEM_DQ8	AC20	MEM_DQ8
MEM_DQ9	AD19	MEM_DQ9
MEM_DQ10	AE22	MEM_DQ10
MEM_DQ11	AC18	MEM_DQ11
MEM_DQ12	AB20	MEM_DQ12
MEM_DQ13	AD22	MEM_DQ13
MEM_DQ14	AC22	MEM_DQ14
MEM_DQ15	AD21	MEM_DQ15
MEM_DQS_P0	Y17	MEM_DQS_P0
MEM_DQS_N0	W18	MEM_DQS_N0
MEM_DQS_P1	AD20	MEM_DQS_P1
MEM_DQS_N1	AE21	MEM_DQS_N1
MEM_DM0	W17	MEM_DM0
MEM_DM1	AE19	MEM_DM1
MEM_DM0(1NC)	AE23	+1.8V_IOPLLVDD
MEM_DM1(1NC)	AE24	+NB_IOPLLVDD
MEM_DQ0(1NC)	AD23	
MEM_DQ1(1NC)	AE18	+MEM_VREF1

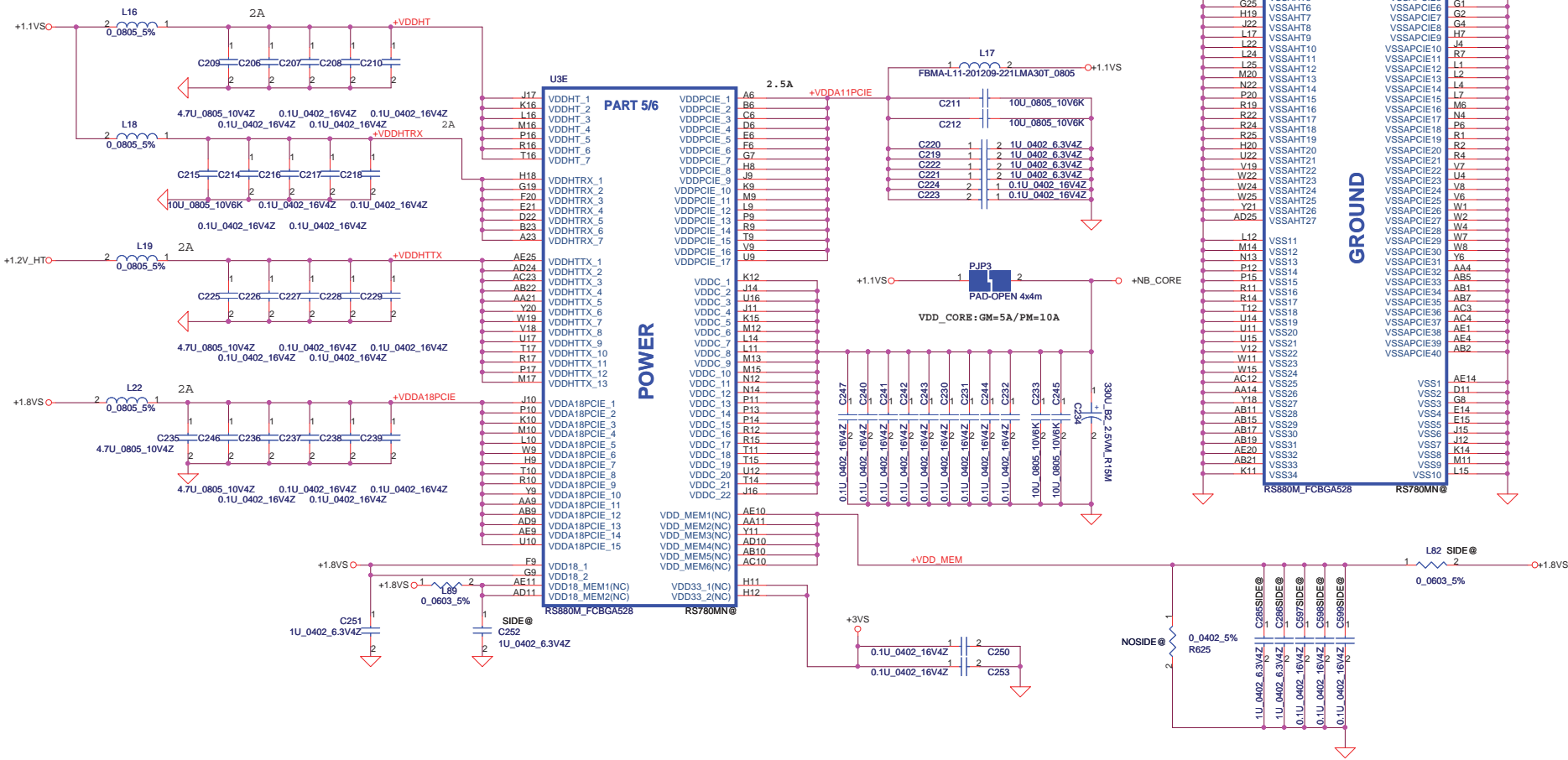


U81		
MEM_BA0	L2	BA0
MEM_BA1	BA1	BA1
MEM_A12	R2	A12
MEM_A11	P7	A11
MEM_A10	M2	A10
MEM_A9	P3	A10/AP
MEM_A8	P8	A8
MEM_A7	P2	A7
MEM_A6	N7	A6
MEM_A5	N3	A5
MEM_A4	N8	A4
MEM_A3	N2	A3
MEM_A2	N7	A2
MEM_A1	M3	A1
MEM_A0	M8	A0
MEM_DQ15	B0	DQ15
MEM_DQ11	D9	DQ11
MEM_DQ10	D1	DQ10
MEM_DQ8	D7	DQ8
MEM_DQ9	C2	DQ9
MEM_DQ14	C8	DQ14
MEM_DQ3	F9	DQ3
MEM_DQ7	F1	DQ7
MEM_DQ1	H8	DQ1
MEM_DQ6	H1	DQ6
MEM_DQ5	H3	DQ5
MEM_DQ0	H7	DQ0
MEM_DQ4	G2	DQ4
MEM_DQ2	G8	DQ2
MEM_DQ0(1NC)	A9	
MEM_DQ1(1NC)	C1	
MEM_DQ3(1NC)	C3	
MEM_DQ7(1NC)	C7	
MEM_DQ9(1NC)	E9	
MEM_DQ14(1NC)	G1	
MEM_DQ11(1NC)	G3	
MEM_DQ10(1NC)	G7	
MEM_DQ8(1NC)	G9	
MEM_DQ6(1NC)	A1	
MEM_DQ5(1NC)	E1	
MEM_DQ3(1NC)	J9	
MEM_DQ1(1NC)	M9	
MEM_DQ0(1NC)	R1	
MEM_DQ15(1NC)	J1	
MEM_DQ11(1NC)	J7	
MEM_DQ10(1NC)	A7	
MEM_DQ8(1NC)	B2	
MEM_DQ9(1NC)	B8	
MEM_DQ14(1NC)	D2	
MEM_DQ3(1NC)	D8	
MEM_DQ7(1NC)	E7	
MEM_DQ1(1NC)	F2	
MEM_DQ6(1NC)	F8	
MEM_DQ5(1NC)	H2	
MEM_DQ0(1NC)	H8	
MEM_DQ4(1NC)	A3	
MEM_DQ2(1NC)	E3	
MEM_DQ0(1NC)	J3	
MEM_DQ1(1NC)	J1	
MEM_DQ2(1NC)	P9	
MEM_DQ0(1NC)	VSS	
MEM_DQ1(1NC)	VSS	
MEM_DQ2(1NC)	VSS	
MEM_DQ3(1NC)	VSS	
MEM_DQ4(1NC)	VSS	
MEM_DQ5(1NC)	VSS	
MEM_DQ6(1NC)	VSS	
MEM_DQ7(1NC)	VSS	
MEM_DQ8(1NC)	VSS	
MEM_DQ9(1NC)	VSS	
MEM_DQ10(1NC)	VSS	
MEM_DQ11(1NC)	VSS	
MEM_DQ12(1NC)	VSS	
MEM_DQ13(1NC)	VSS	
MEM_DQ14(1NC)	VSS	
MEM_DQ15(1NC)	VSS	
MEM_DQS_P0(1NC)	VSS	
MEM_DQS_N0(1NC)	VSS	
MEM_DQS_P1(1NC)	VSS	
MEM_DQS_N1(1NC)	VSS	
MEM_DM0(1NC)	VSS	
MEM_DM1(1NC)	VSS	
MEM_ODT(1NC)	VSS	
MEM_CLKP(1NC)	VSS	
MEM_CLKN(1NC)	VSS	
MEM_CAS#(1NC)	VSS	
MEM_WE#(1NC)	VSS	
MEM_CS#(1NC)	VSS	
MEM_RAS#(1NC)	VSS	
MEM_CKE(1NC)	VSS	
MEM_BA2(1NC)	VSS	
MEM_BA1(1NC)	VSS	
MEM_BA0(1NC)	VSS	
MEM_A12(1NC)	VSS	
MEM_A11(1NC)	VSS	
MEM_A10(1NC)	VSS	
MEM_A9(1NC)	VSS	
MEM_A8(1NC)	VSS	
MEM_A7(1NC)	VSS	
MEM_A6(1NC)	VSS	
MEM_A5(1NC)	VSS	
MEM_A4(1NC)	VSS	
MEM_A3(1NC)	VSS	
MEM_A2(1NC)	VSS	
MEM_A1(1NC)	VSS	
MEM_A0(1NC)	VSS	

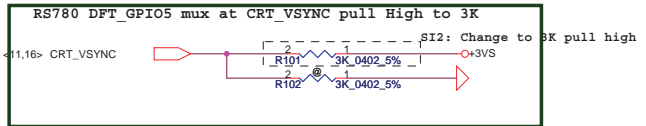


U61 SAMSIDE@ K4N1G164QE-HC20
SA00002UH00 : Hynix
SA000031O00 : Samsung
64M*16 DDR2 400MHZ

Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	RS780M&RX781 SIDE PORT
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Date:	Friday, April 10, 2009	Sheet	13 of 46



DFT_GPIO5:STRAP_DEBUG_BUS_GPIO_ENABLEb

Enables the Test Debug Bus using GPIO.

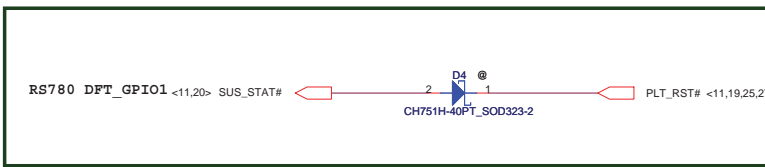
1 : Enable (RX780, RS780)
 0 : Disable (RX780, RS780)
 PIN: RS740-->RS780_AUX_CAL; RX780-->NB_TV_C; RS780--> VSYNC#

RS780 use register to control PCI-E configure

DFT_GPIO[4:2]: STRAP_PCIE_GPP_CFG[2:0]

These pin straps are used to configure PCI-E GPP mode.

000 : 00001
 001 : 00010
 010 : 01011
 011 : 00100
 100 : 01010
 101 : 01100
 111 : 01011

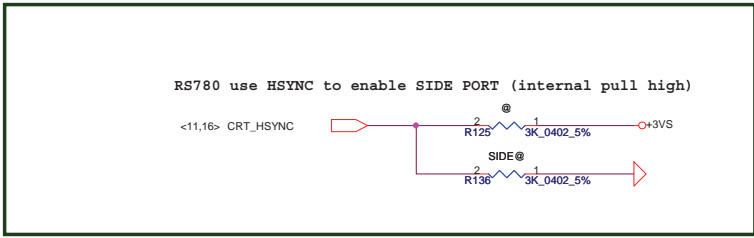


DFT_GPIO1: LOAD_EEPROM_STRAPS

Selects Loading of STRAPS from EPROM

1 : Bypass the loading of EEPROM straps and use Hardware Default Values
 0 : I2C Master can load strap values from EEPROM if connected, or use default values if not connected

RS740/RX780: DFT_GPIO1 RS780:SUS_STAT



DFT_GPIO0: STRAP_DEBUG_BUS_PCIE_ENABLEb

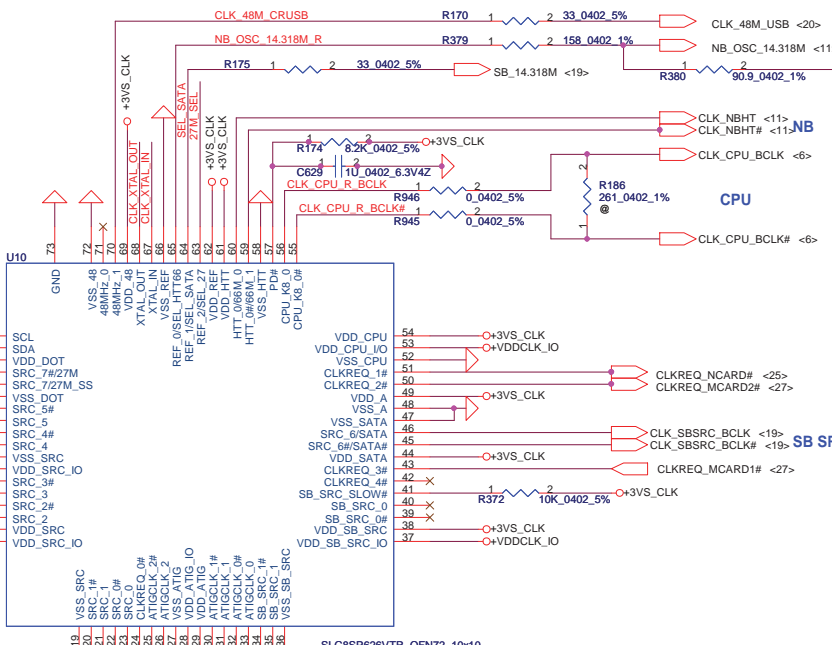
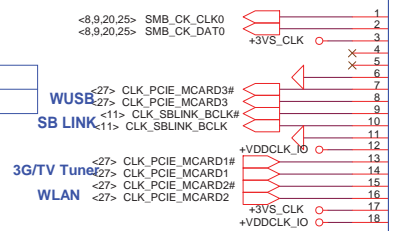
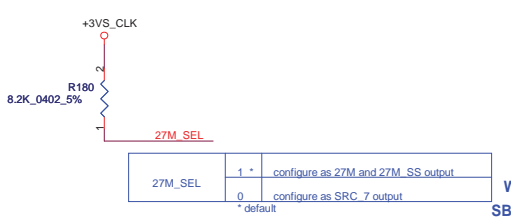
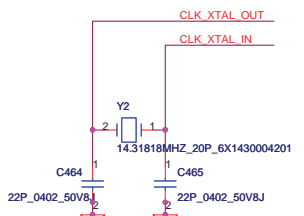
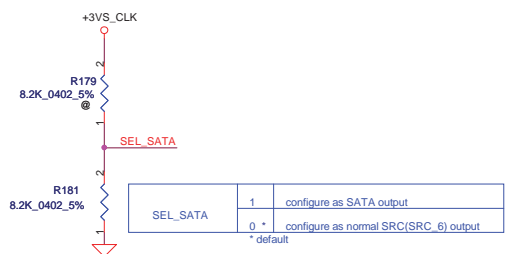
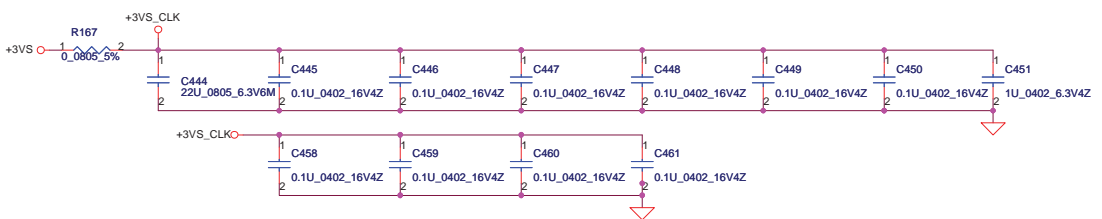
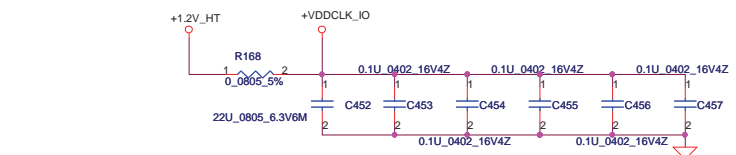
RX780: Enables the Test Debug Bus using PCIE bus

1 : Disable (Can still be enabled using nbcfg register access)
 0 : Enable

RS780: Enables Side port memory (RS780 use HSYNC#)

1. Disable (RS780)
 0 : Enable (RS780)

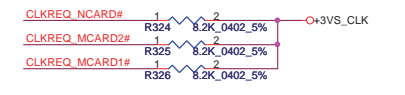
Security Classification	Compal Secret Data			Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Compal Electronics, Inc.	
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		OSC_14M_NB
RS780	1	1.1V 158R/90.9R

Use voltage divider resistor R379 & R380 to pull low

NB_OSC_14.318M	1	configure as single-ended 66MHz output
	0 *	configure as differential 100MHz output
		* default



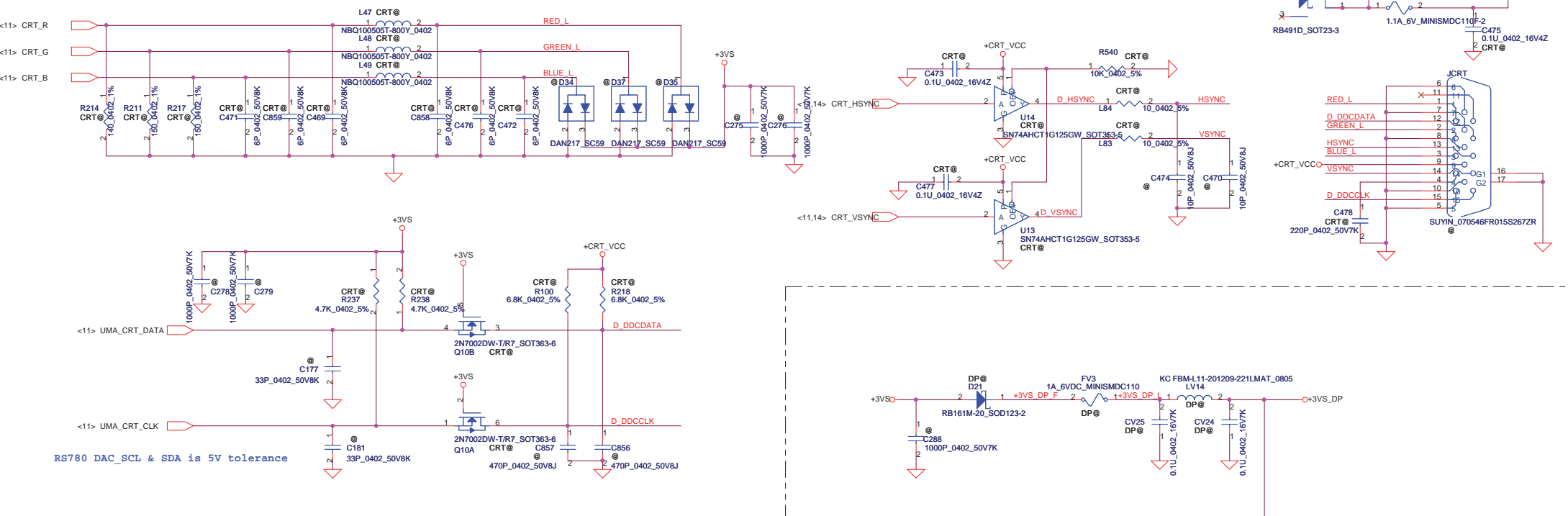
NB CLOCK INPUT TABLE

NB CLOCKS	RX780	RS780
HT_REFCLKP	100M DIFF	100M DIFF
HT_REFCLKN	100M DIFF	100M DIFF
REFCLK_P	14M_SE (1.8V)	14M_SE (1.1V)
REFCLK_N	NC	vref
GFX_REFCLK	100M DIFF	100M DIFF(IN/OUT)*
GPP_REFCLK	100M DIFF	NC or 100M DIFF OUTPUT
GPPSB_REFCLK	100M DIFF	100M DIFF

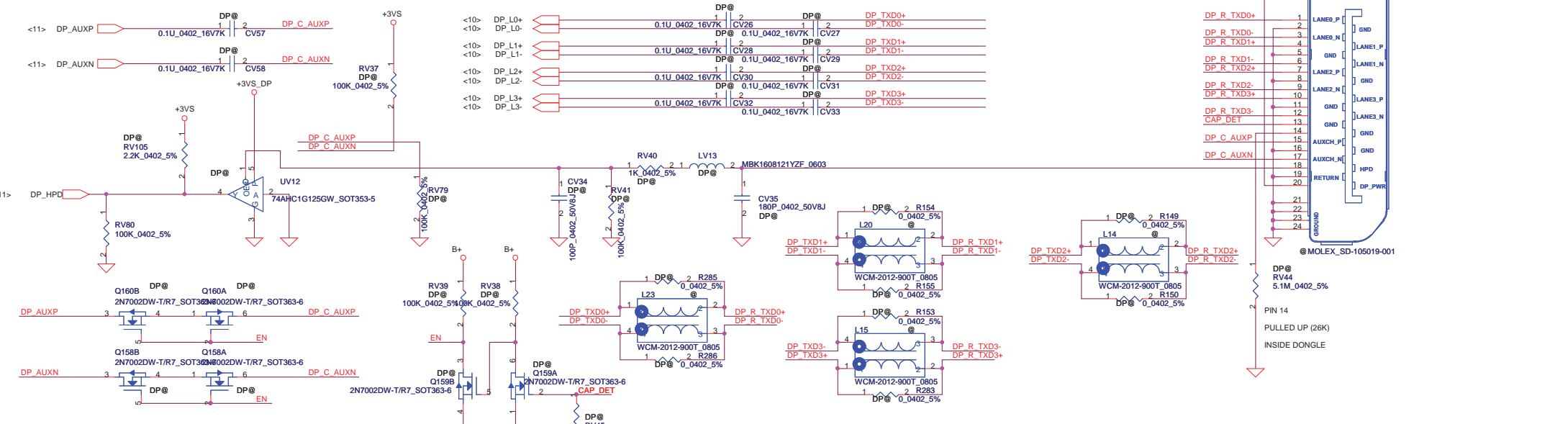
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Issued Date	2008/04/14	Deciphered Date
		2009/04/14
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Title		Compal Electronics, Inc.	
		Clock Generator	
Document Number	LA-538IP		Rev
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Date:	Friday, April 10, 2009	Sheet	15 of 46

CRT CONNECTOR



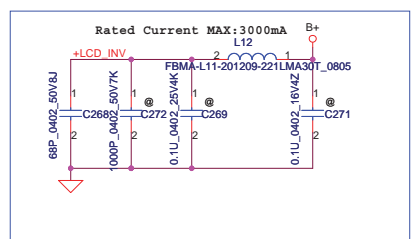
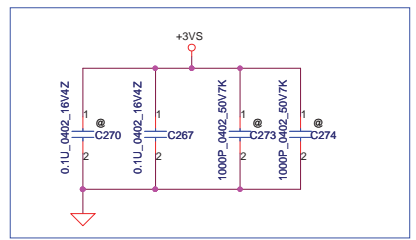
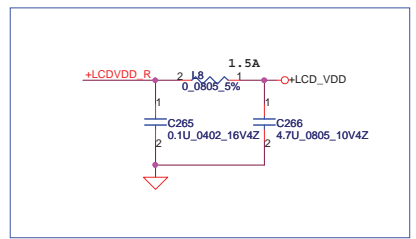
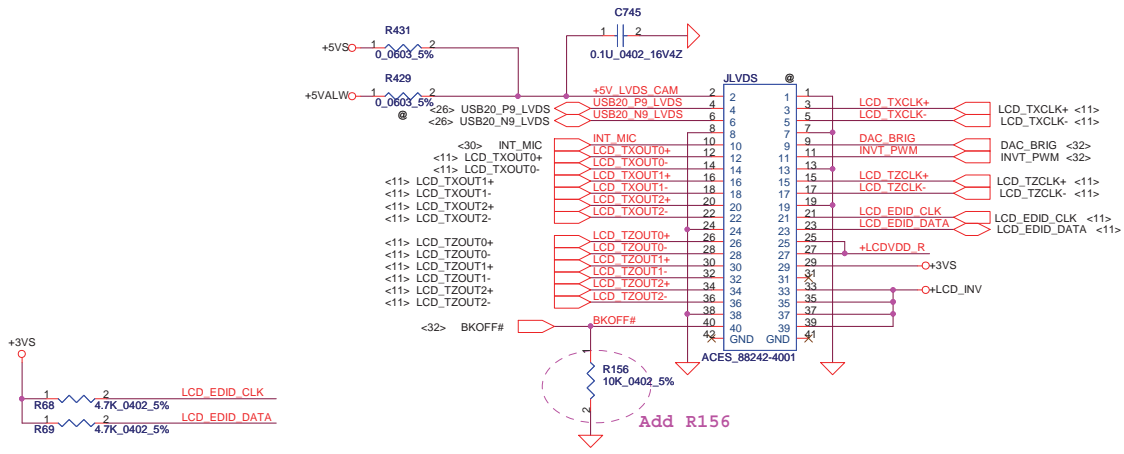
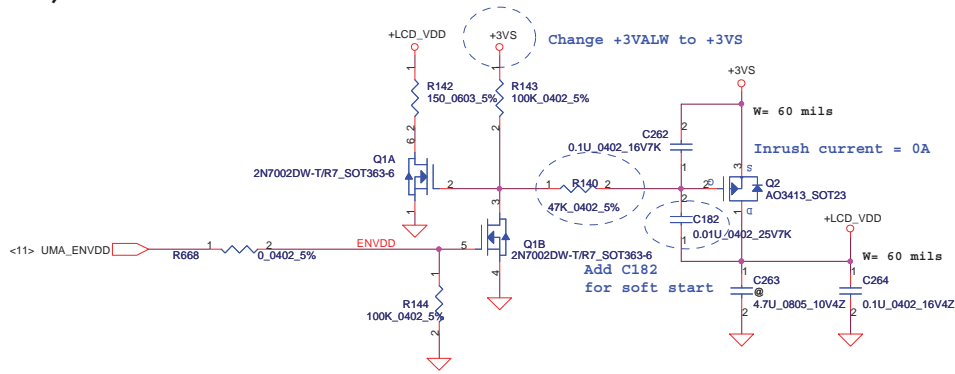
Display Port



<http://hobi-elektronika.net>

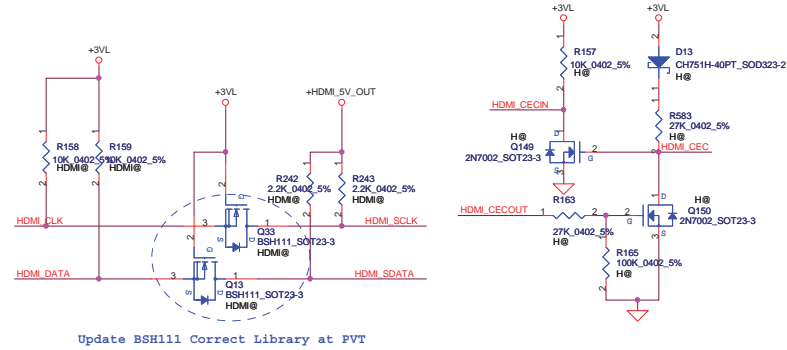
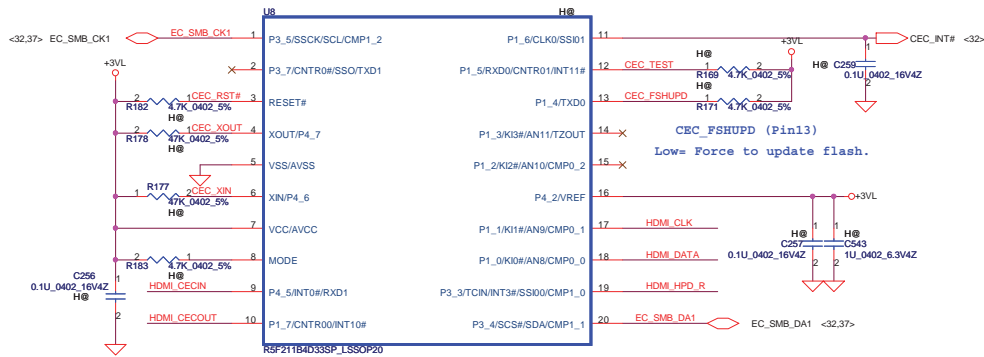
Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	Compal Electronics, Inc.
				CRT/TV-OUT Connector
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LCD/PANEL BD. Conn.

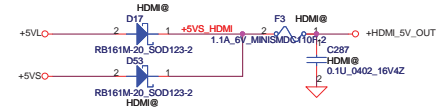
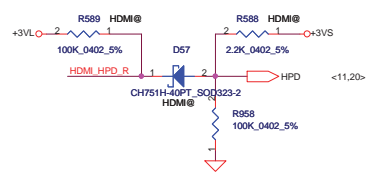


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Issued Date	2008/04/14	Deciphered Date	2009/04/14	LCD CONN.	
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				LA-538IP	0.2
Date: Friday, April 10, 2009				Sheet	17 of 46

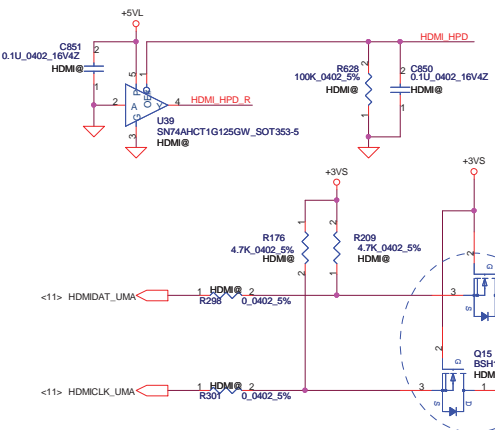
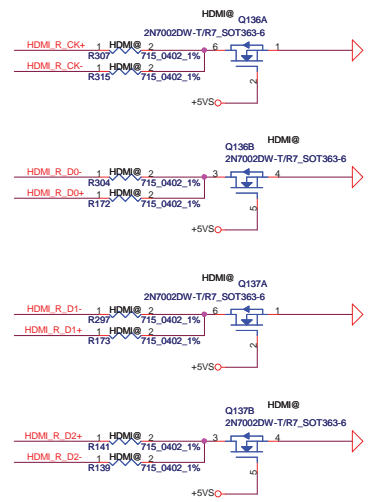
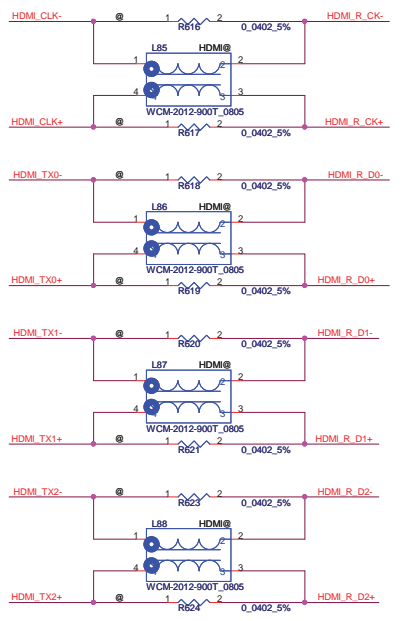
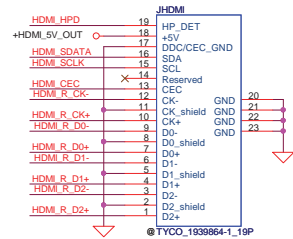
HDMI CEC Controller



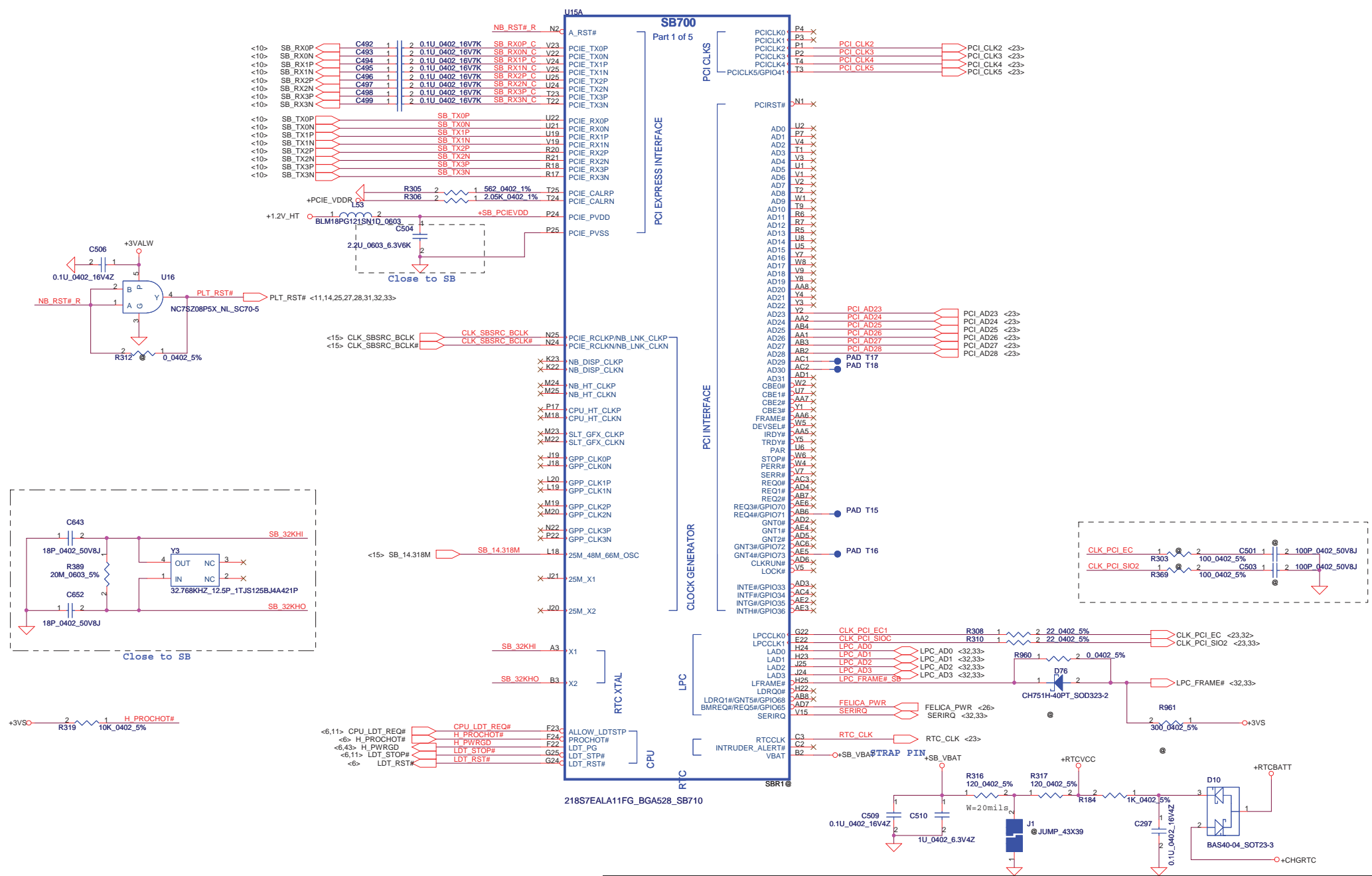
Update BSH11 Correct Library at PVT



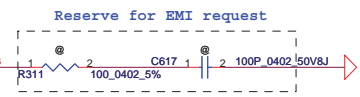
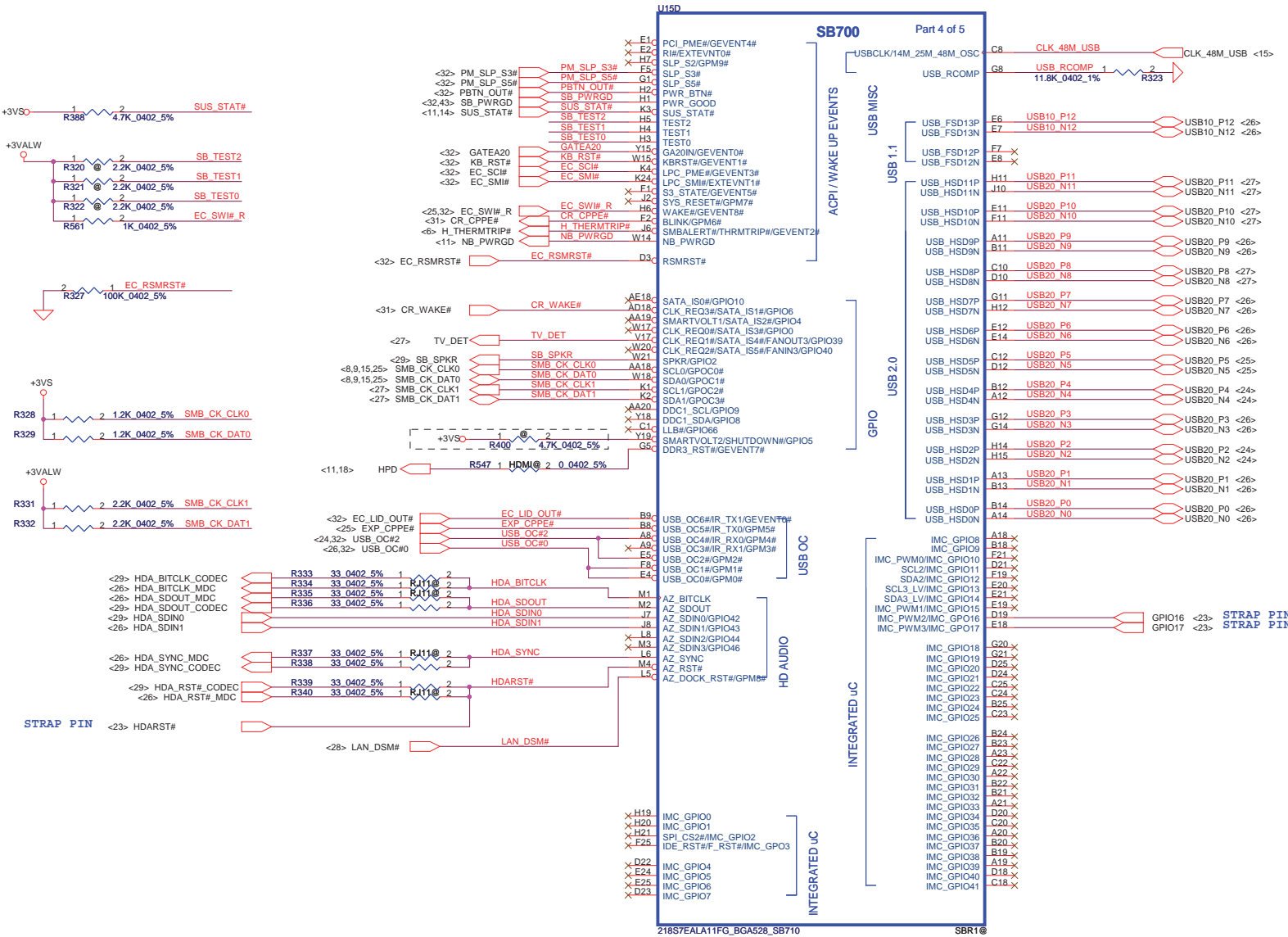
HDMI Connector



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Issued Date	2008/04/14	Deciphered Date	2009/04/14	HDMI/CEC	
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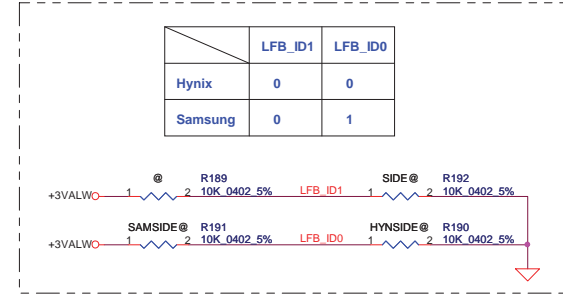
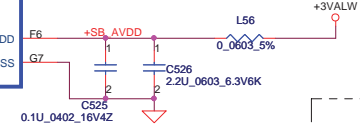
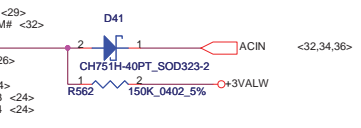
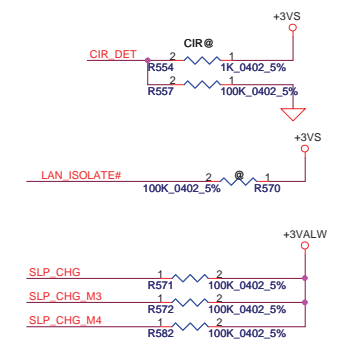
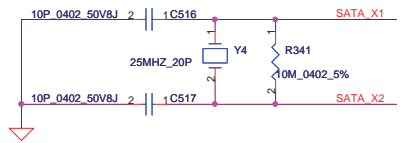
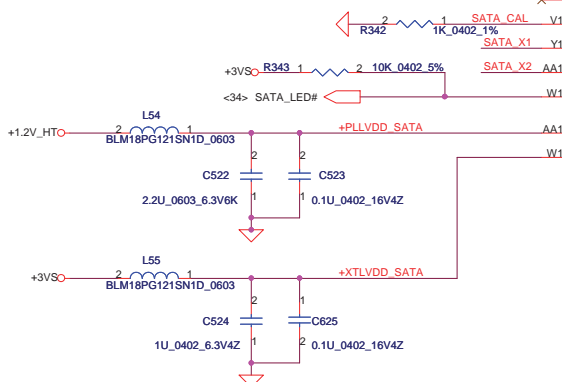
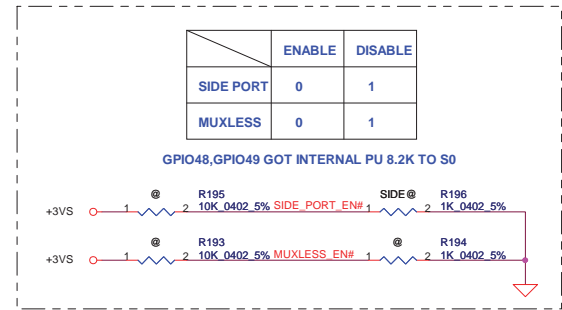
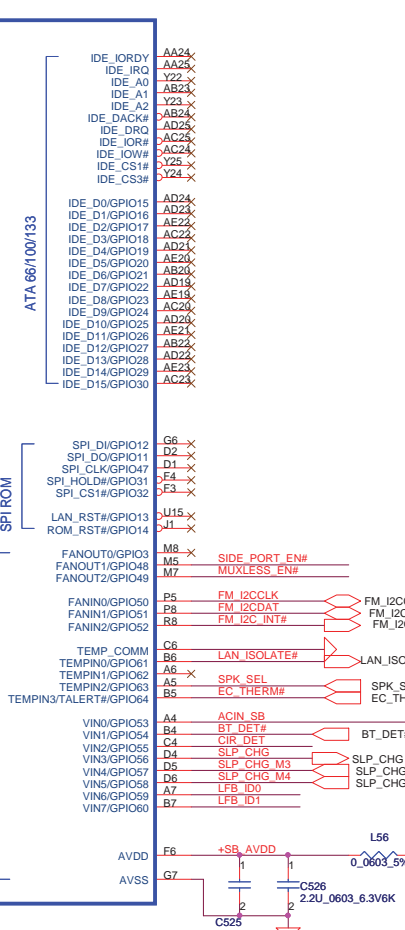
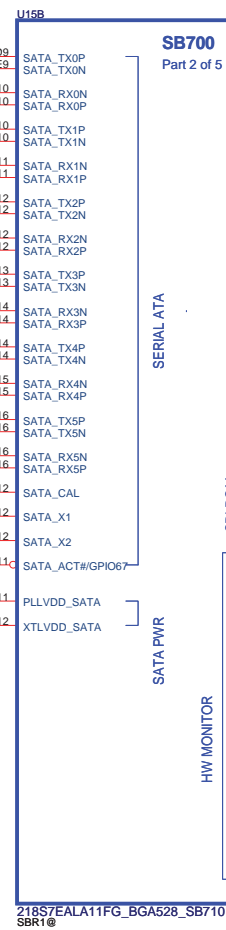
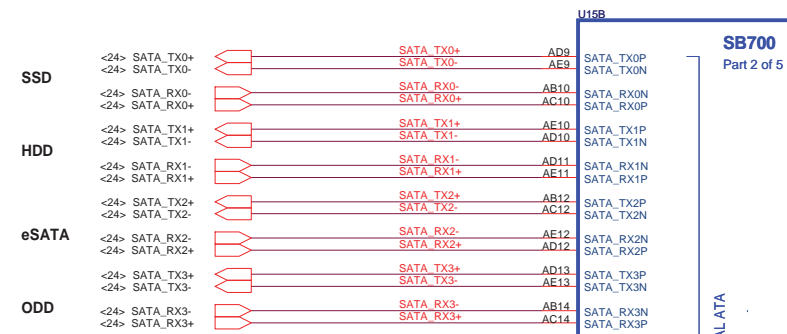


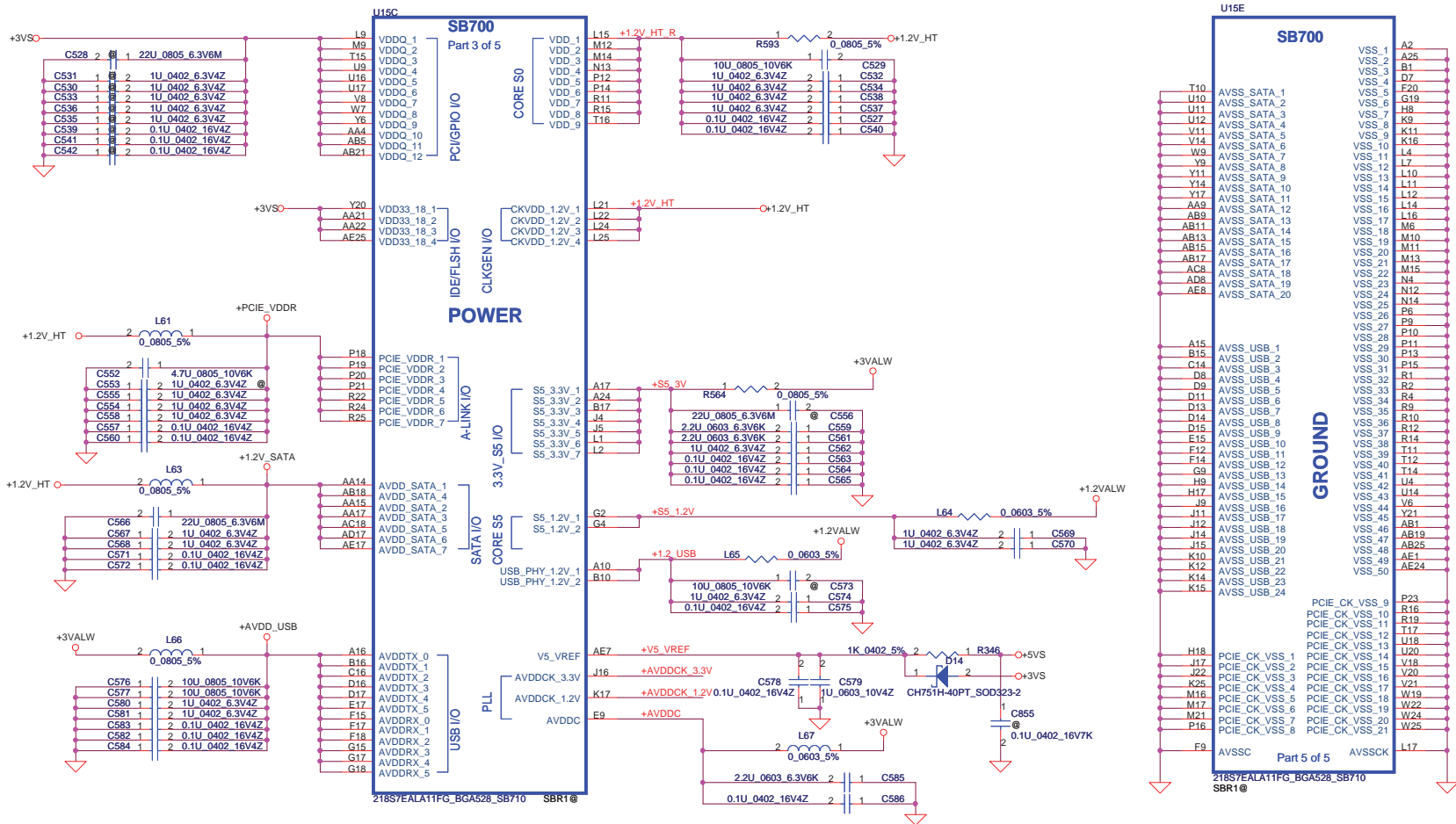
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Issued Date	2008/04/14	Deciphered Date	2009/04/14
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- USB-13 Touch Screen
- Swap USB port 5 and port 11 for TV tuner issue
- USB-11 TV Tuner
- USB-10 GPS
- USB-9 Int Camera
- USB-8 WiFi
- USB-7 Finger Printer
- USB-6 Bluetooth
- USB-5 New Card
- USB-4 Left side
- USB-3 Felica
- USB-2 eSATA
- USB-1 Right side
- USB-0 Right side

Security Classification		Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	SB700 USB/AC97	
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				LA-538IP	0.2
Date: Friday, April 10, 2009				Sheet	20 of 46



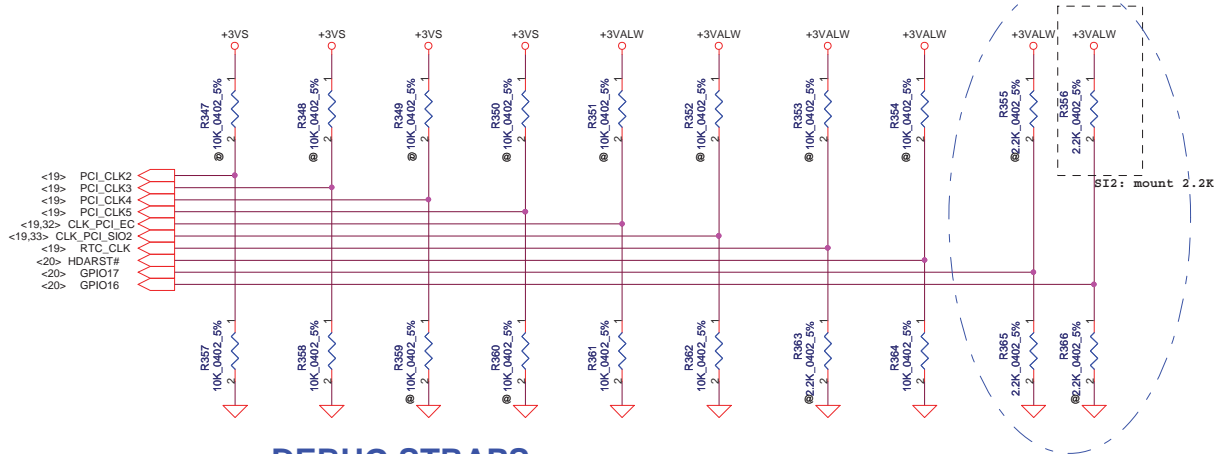


Security Classification	Compal Secret Data		Title	
Issued Date	2008/04/14	Deciphered Date	2009/04/14	SB700 Power/GND
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REQUIRED STRAPS

NOTE: SB700 HAS INTERNAL 15K PULL UP RESISTOR FOR RTC_CLK

	PCI_CLK2	PCI_CLK3	PCI_CLK4	PCI_CLK5	LPC_CLK0	LPC_CLK1	RTC_CLK	AZ_RST_CD#	GP17	GP16
PULL HIGH	BOOTFAIL TIMER ENABLED	USE DEBUG STRAPS	RESERVED	RESERVED	ENABLE PCI MEM BOOT	CLKGEN ENABLED	INTERNAL RTC DEFAULT	EC ENABLED	Internal pull up H,H = Reserved H,L = SPI ROM	
PULL LOW	BOOTFAIL TIMER DISABLED DEFAULT	IGNORE DEBUG STRAPS DEFAULT			DISABLE PCI MEM BOOT DEFAULT	CLKGEN DISABLED DEFAULT	EXT. RTC (PD on X1, apply 32KHz to RTC_CLK)	EC DISABLED DEFAULT		L,H = LPC ROM (Default) L,L = FWH ROM

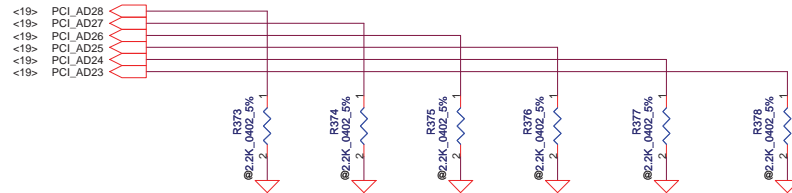


DEBUG STRAPS

SB700 HAS 15K INTERNAL PU FOR PCI_AD[28:23]

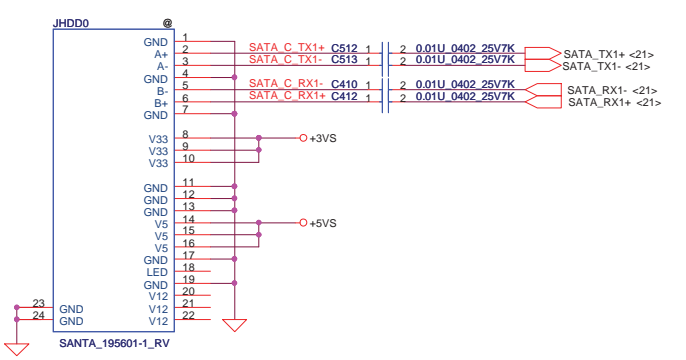
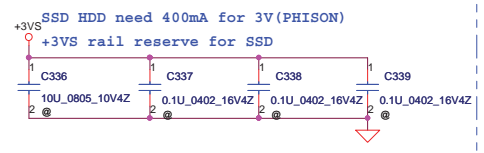
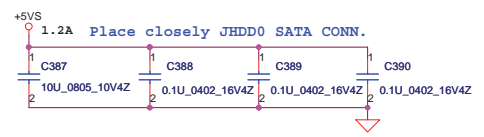
Need to confirm if SB SPI ROM will mount

	PCI_AD28	PCI_AD27	PCI_AD26	PCI_AD25	PCI_AD24	PCI_AD23
PULL HIGH	USE LONG RESET DEFAULT	USE PCI PLL DEFAULT	USE ACPI BCLK DEFAULT	USE IDE PLL DEFAULT	USE DEFAULT PCIE STRAPS DEFAULT	RESERVED
PULL LOW	USE SHORT RESET	BYPASS PCI PLL	BYPASS ACPI BCLK	BYPASS IDE PLL	USE EEPROM PCIE STRAPS	

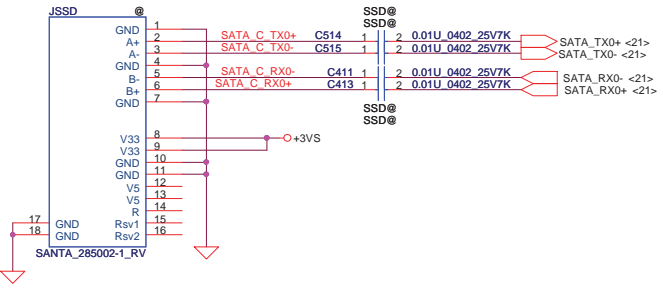
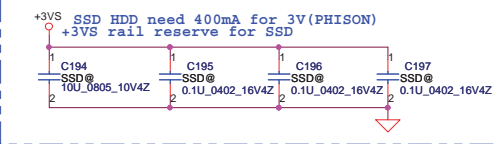


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				Rev		0.2
				Date		Friday, April 10, 2009
				Sheet		23 of 46
				Rev		0.2
				Date		Friday, April 10, 2009
				Sheet		23 of 46
				Rev		0.2

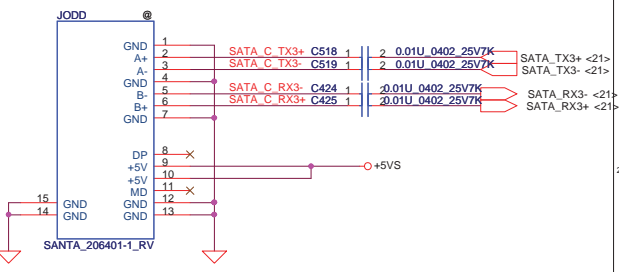
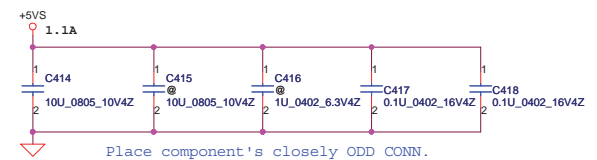
SATA HDDO Conn.



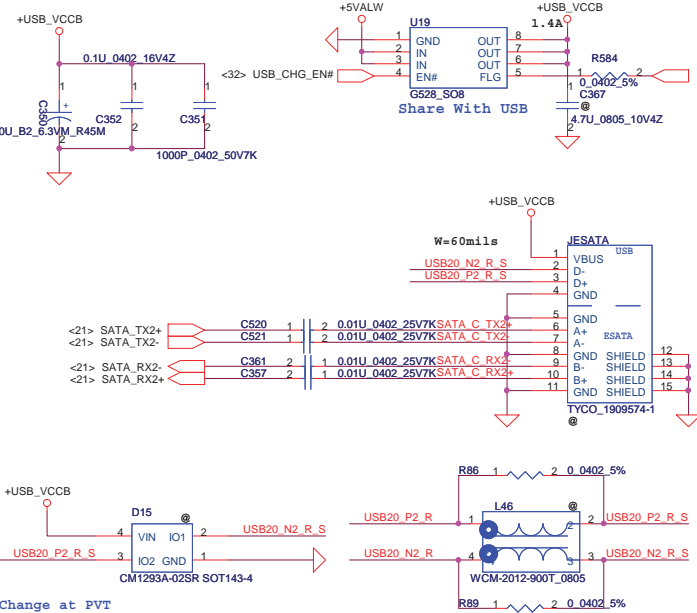
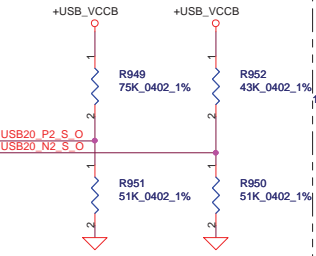
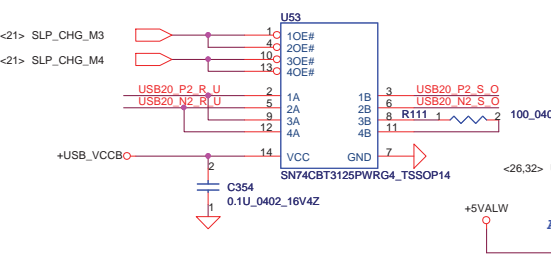
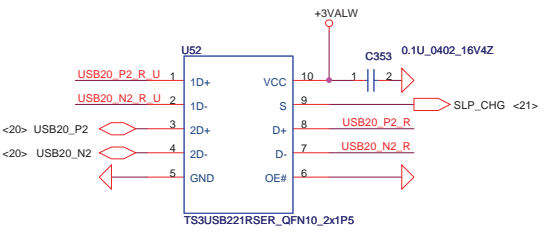
SSD Conn.



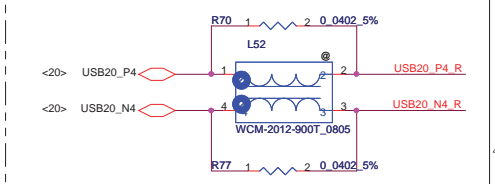
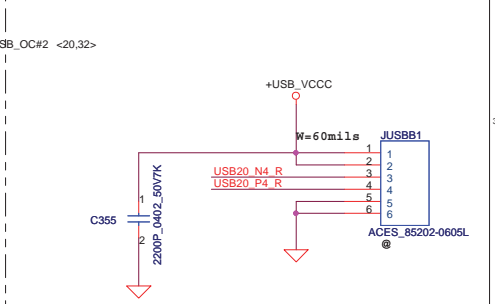
SATA ODD Conn



E-SATA/USB



LEFT USB



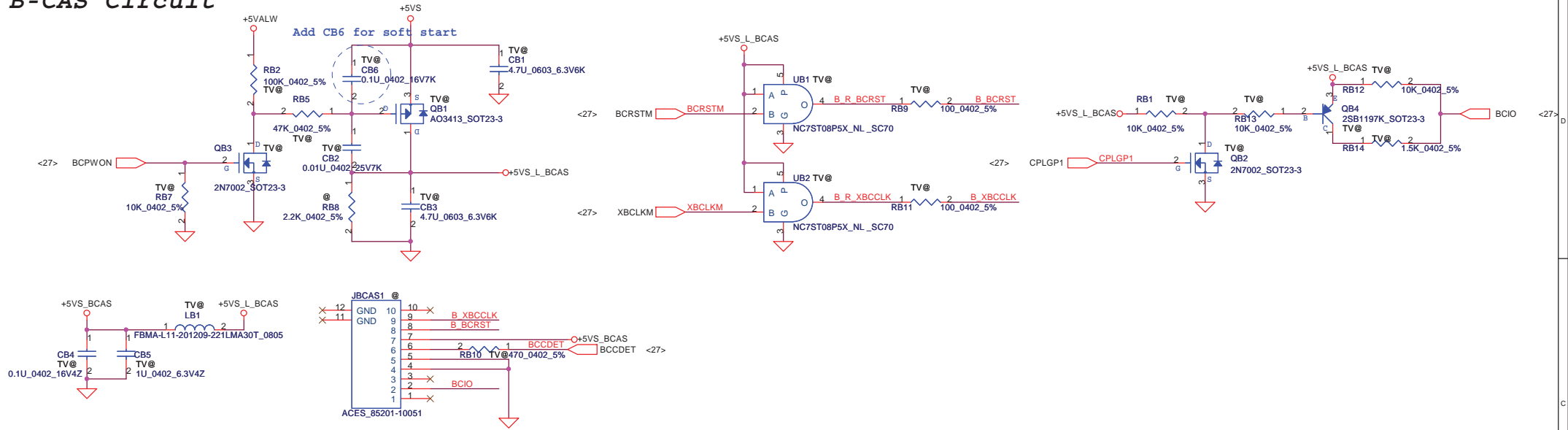
	SLP_CHG_M3	SLP_CHG_M4	SLP_CHG	FUNCTION
Mode 3	HIGH	LOW	LOW	D=1D
Mode 4	LOW	HIGH	HIGH	D=2D

Security Classification	Compal Secret Data	
Issued Date	2008/04/14	Deciphered Date
		2009/04/14

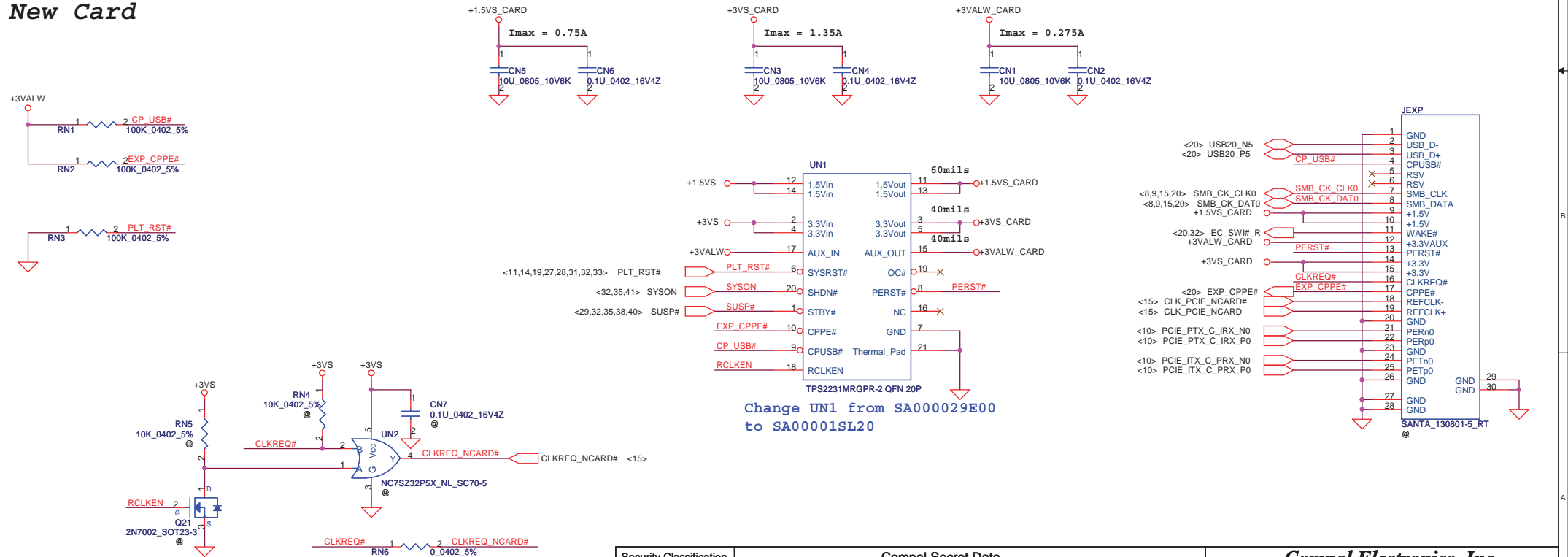
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SATA HDD/ODD		
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B-CAS Circuit

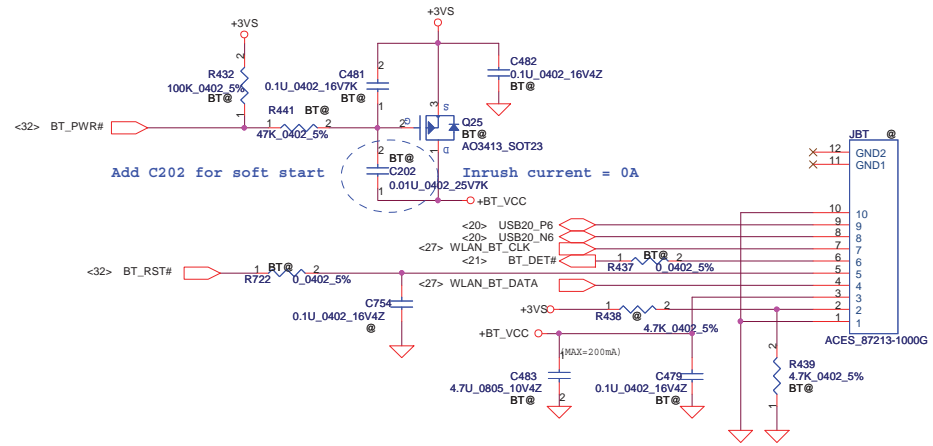


New Card

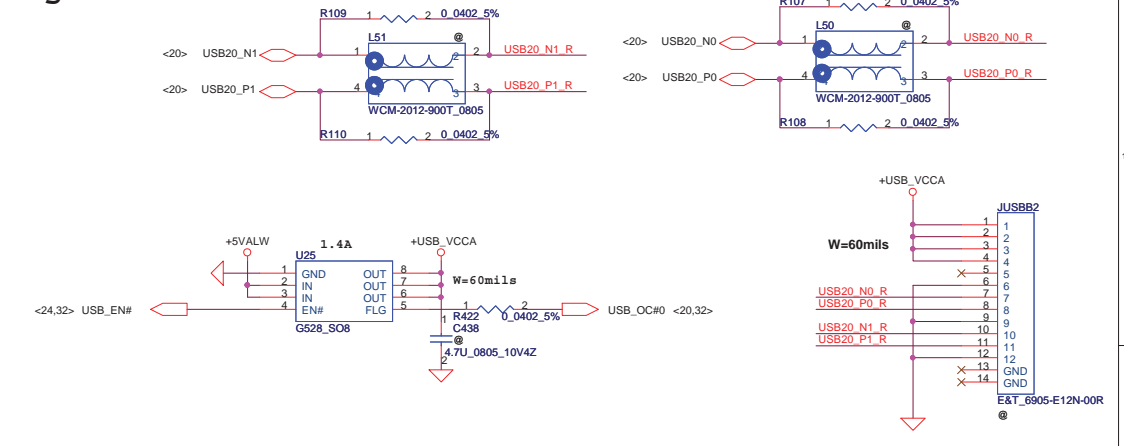


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Issued Date	2008/10/06	Deciphered Date	2009/10/06	eSATA/NEW CARD	
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Size	Document Number	Date		Sheet	Rev
	LA-5381P	Friday, April 10, 2009		25	0.2

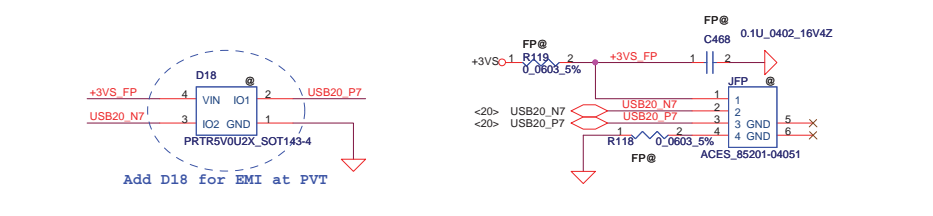
BlueTooth Interface



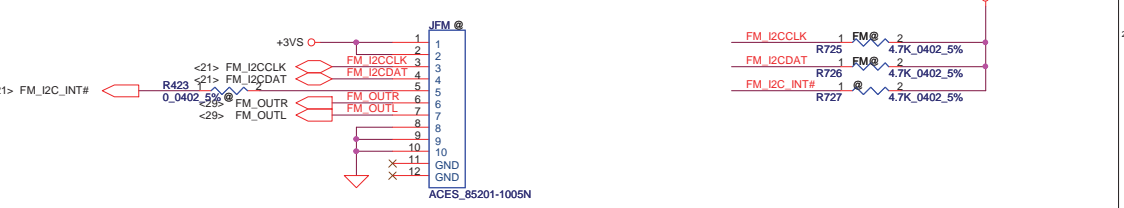
Right USB Board



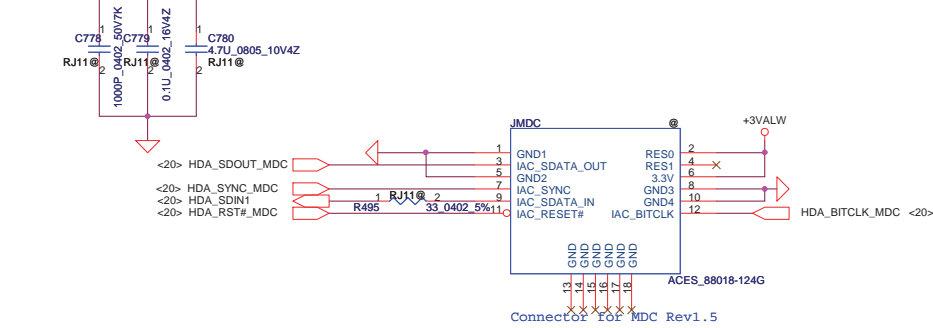
Finger printer



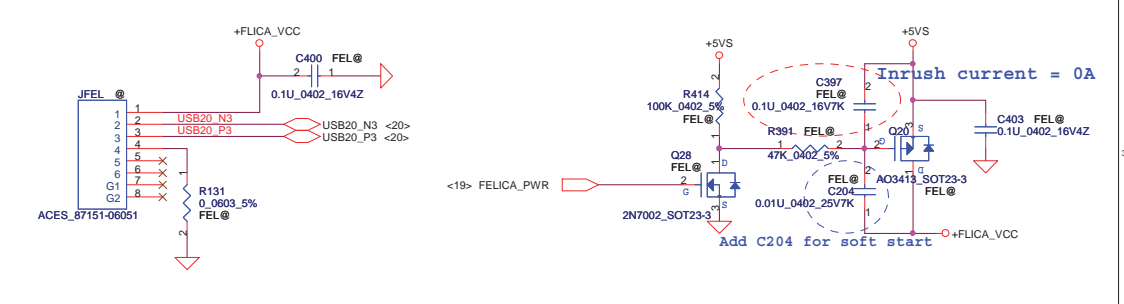
FM Tuner



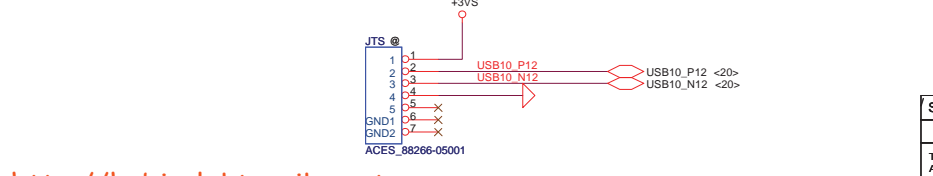
MDC 1.5 Conn.



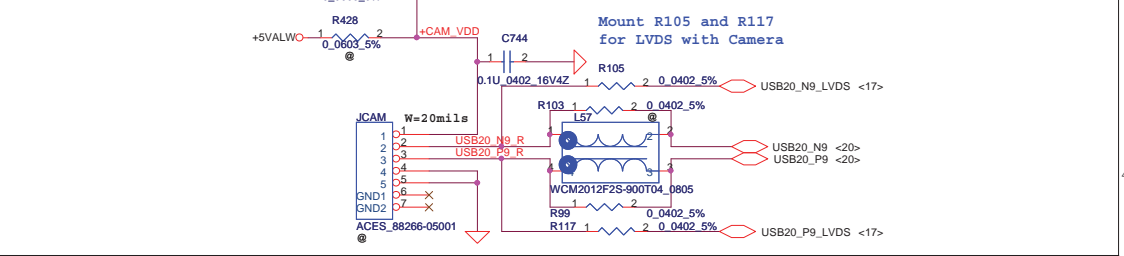
Felica



Touch Screen

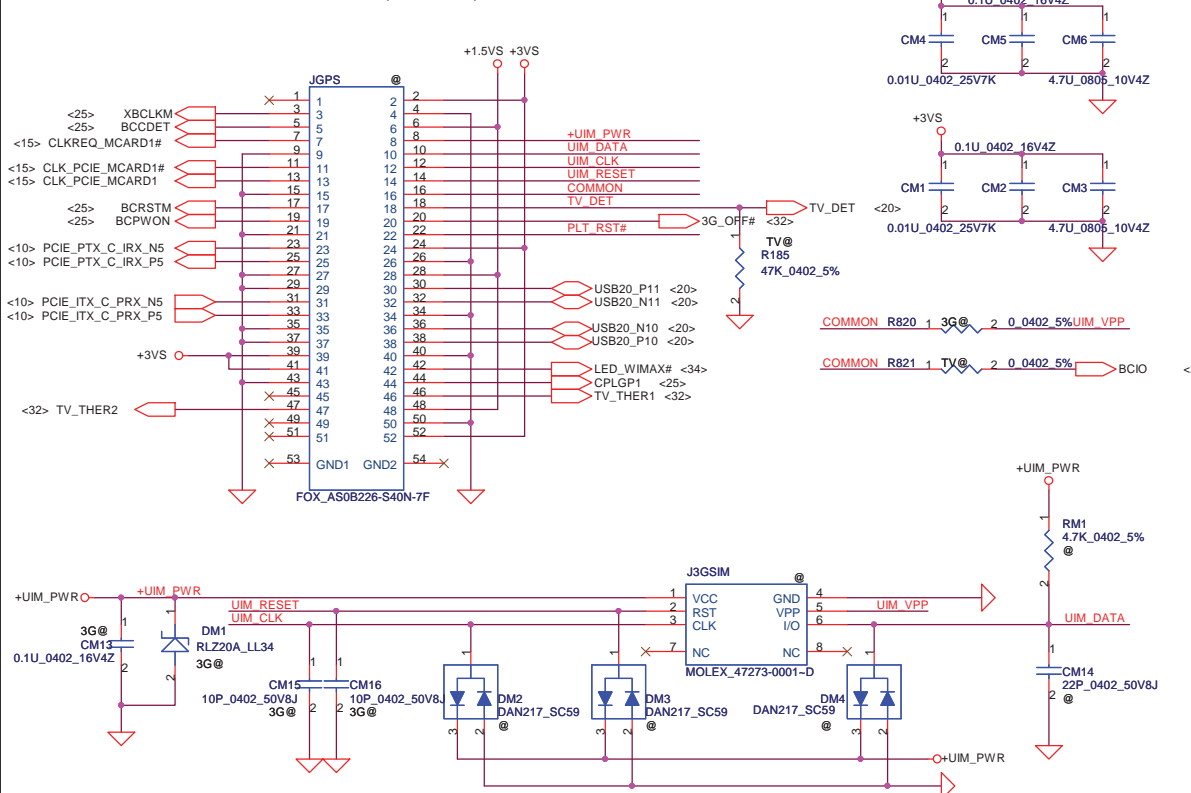


Int. Camera

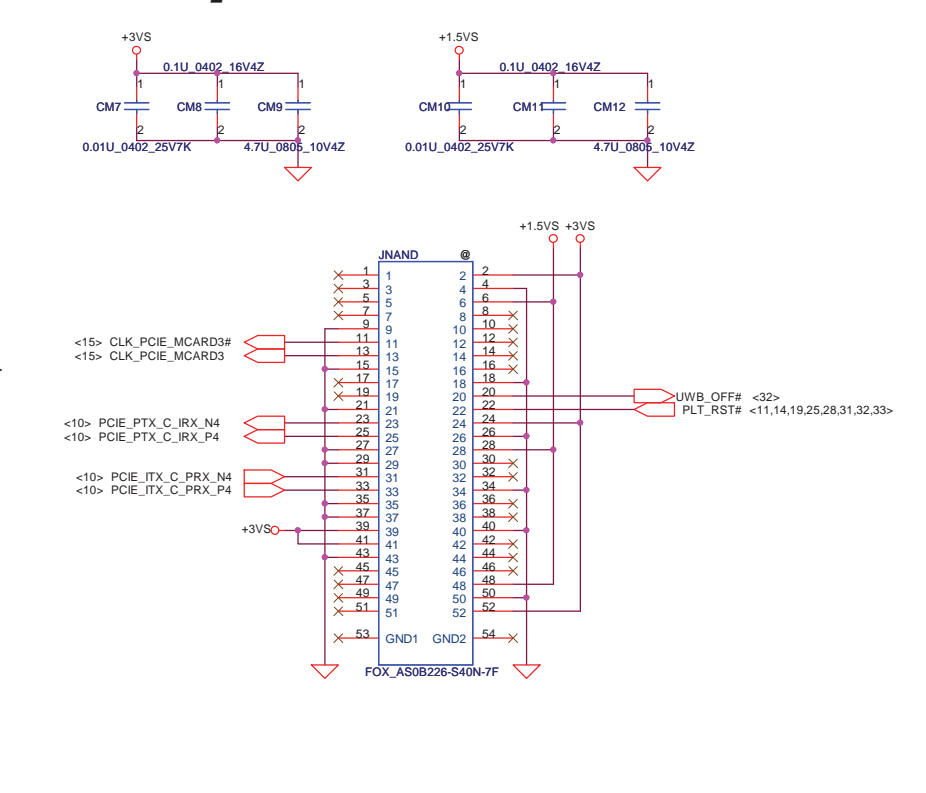


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Issued Date	2008/04/14	Deciphered Date	2009/04/14	USB/BT/FingerPrint
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<p>Document Number LA-5381P</p>			<p>Rev 0.2</p>	
<p>Date: Friday, April 10, 2009 Sheet 26 of 46</p>				

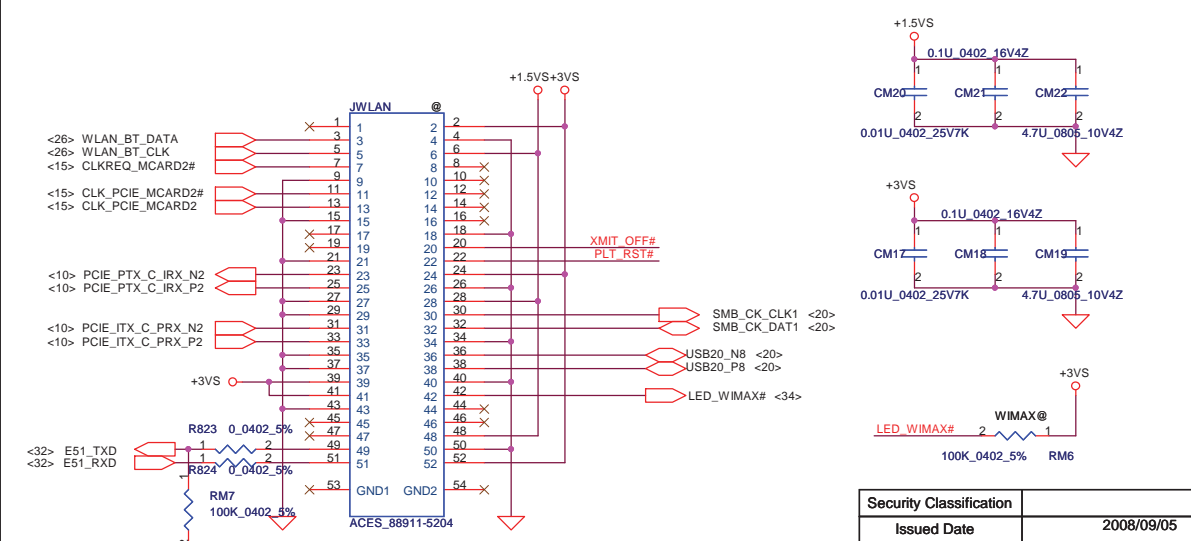
PCIe Mini Card-3G/GPS/TV Tuner (Slot 2)



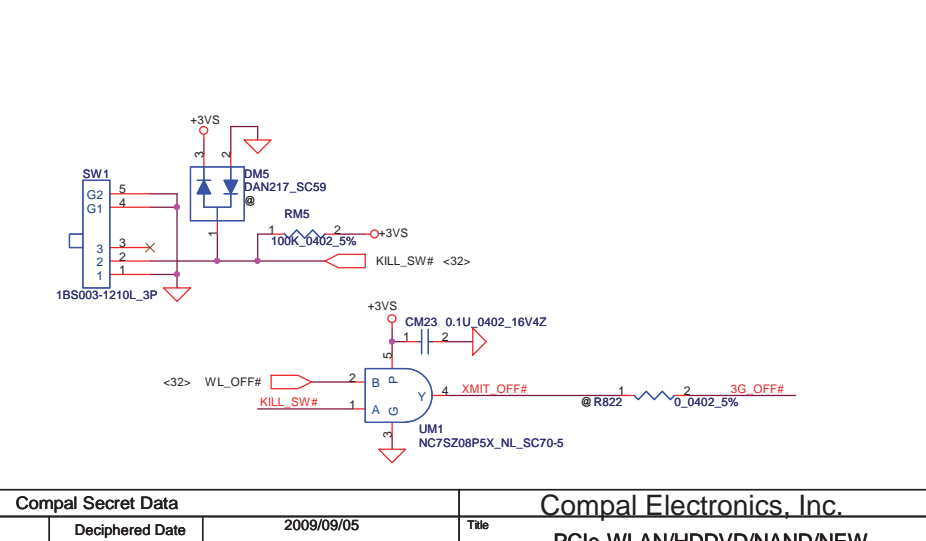
WUSB or Upconvert (Slot 3)



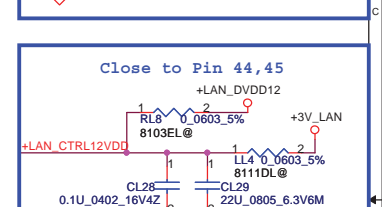
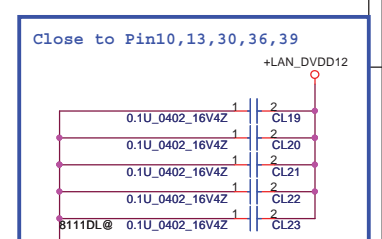
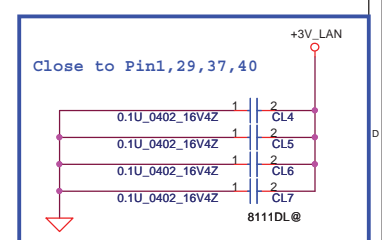
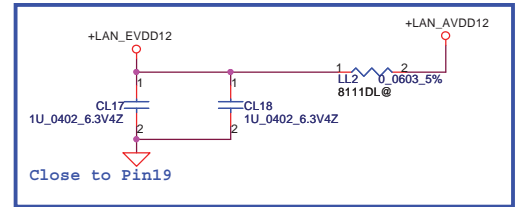
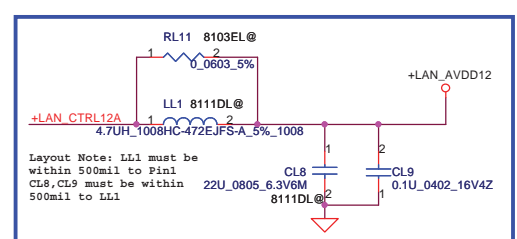
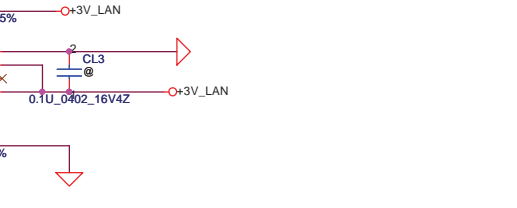
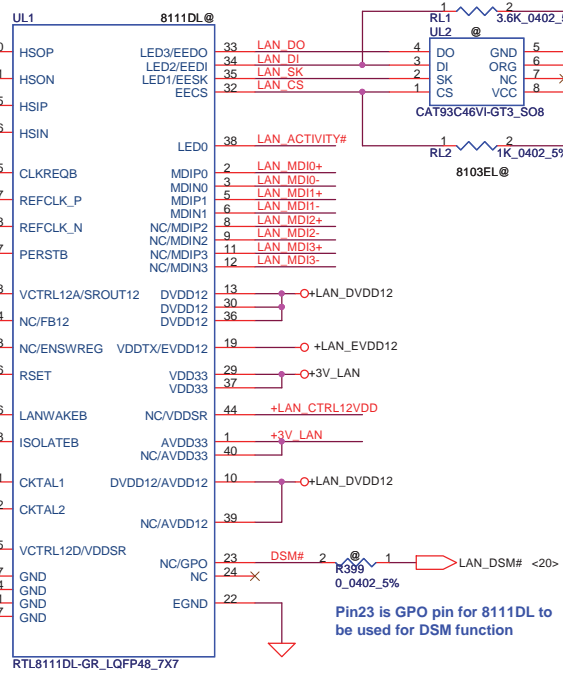
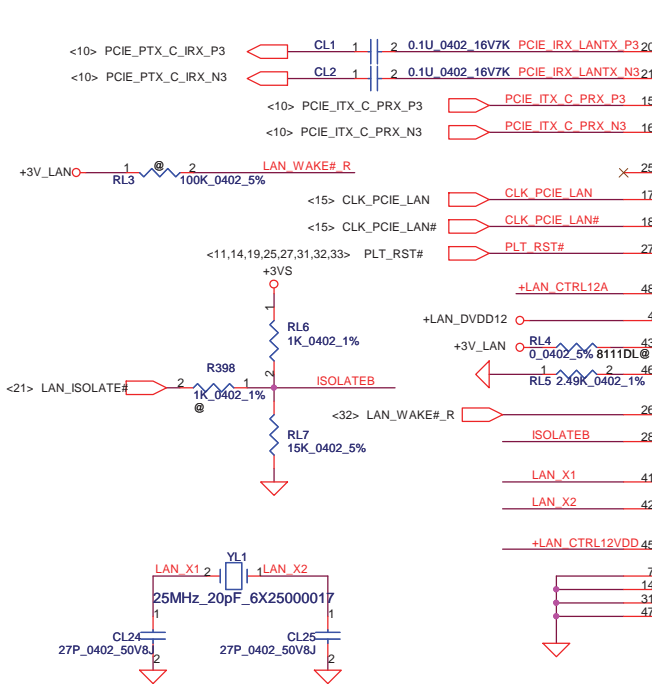
PCIe Mini Card-WLAN/WiMax (Slot 1)



Kill SWITCH

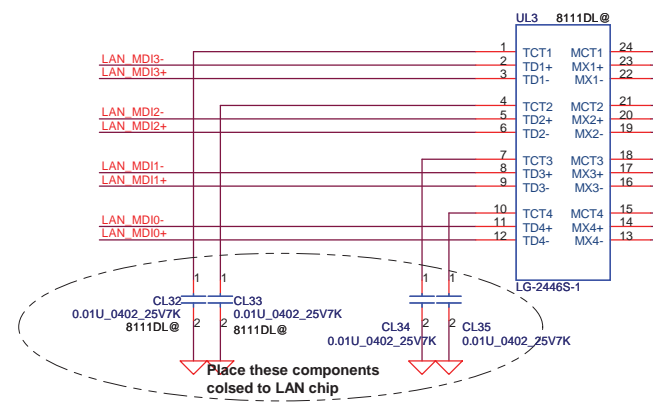


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Issued Date	2008/09/05	Deciphered Date	2009/09/05	Title
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Size	Document Number	Rev		0.2
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Date:	Friday, April 10, 2009	Sheet	27	of 46

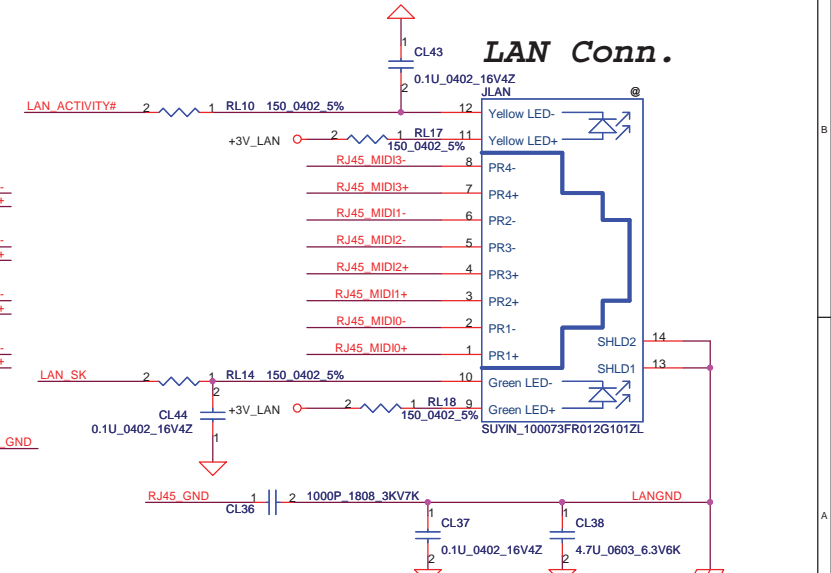


pin assignments table for difference

Pin	8111DL	8103EL
4	FB12	NC
8	MDIP2	NC
9	MDIN2	NC
10	AVDD12	DVDD12
11	MDIP3	NC
12	MDIN3	NC
19	EVDD12	VDDTX
23	GPO	NC
33	EEDO	LED3
34	EBDI	LED2
35	ESK	LED1
39	AVDD12	NC
40	AVDD33	NC
43	ENSR	NC
44	VDDSR	NC
45	VDDSR	VCTRL12D
48	SROUT12	VCTRL12A

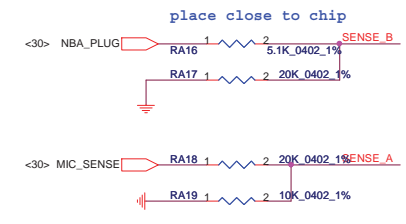
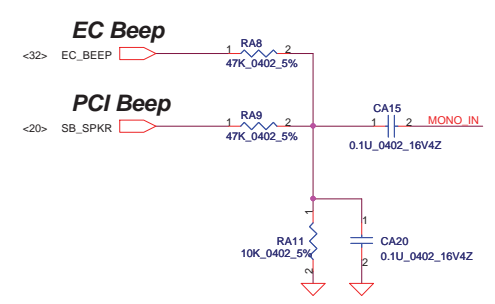
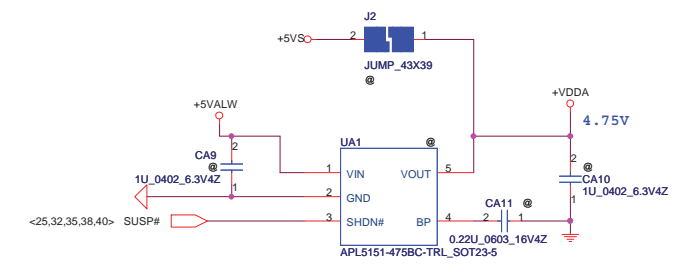
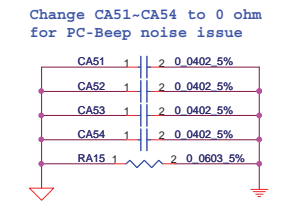
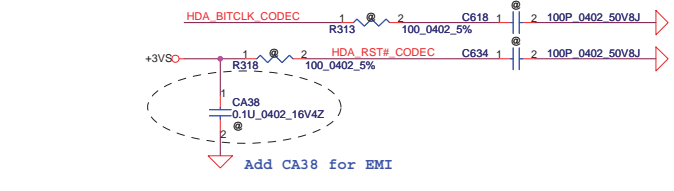
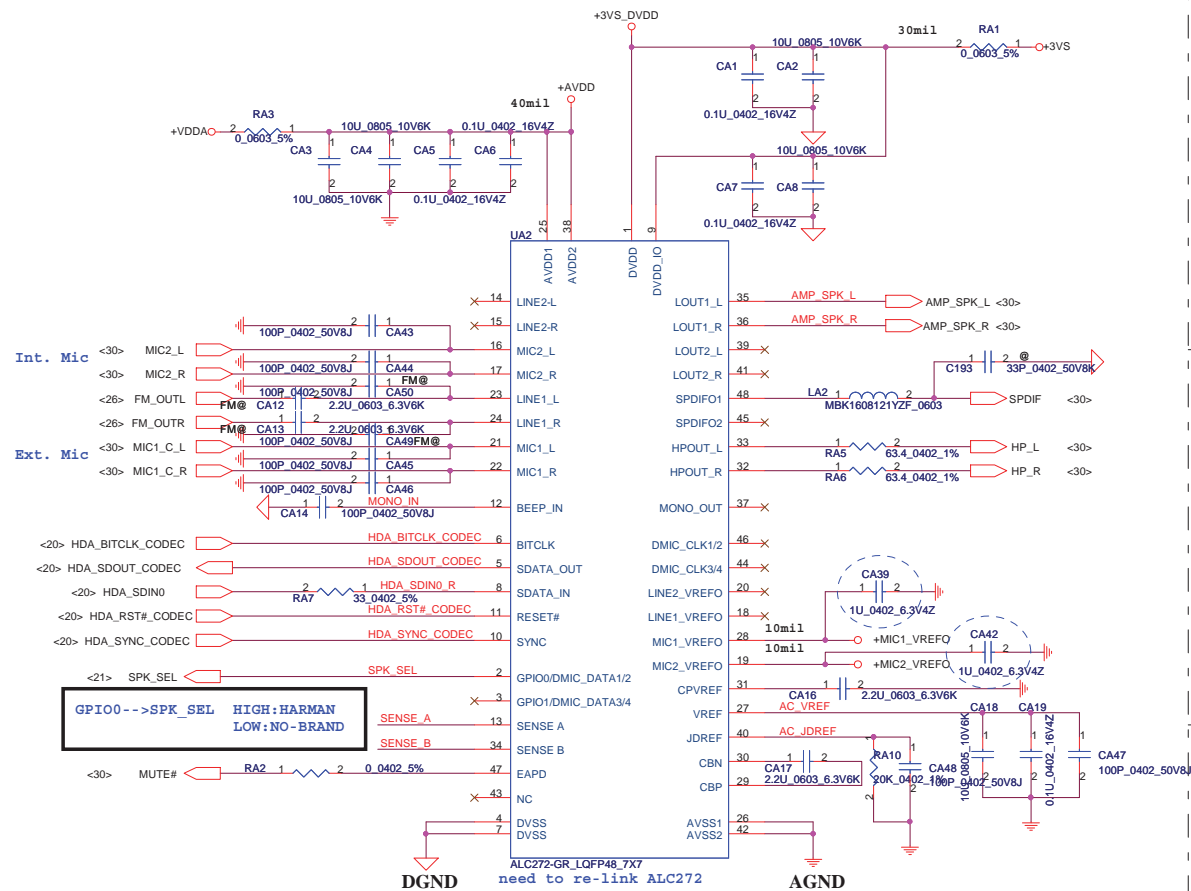


Place these components close to LAN chip



LAN Conn.

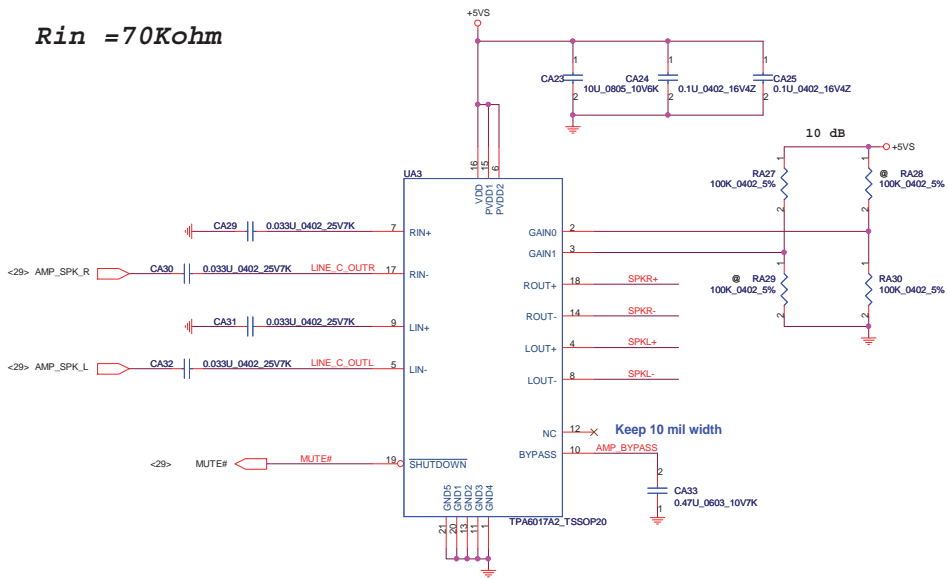
Security Classification		Compal Secret Data		Title	
Issued Date	2008/10/06	Deciphered Date	2009/10/06	RTL8103EL/RTL8111DL	
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				Document Number	
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				Date:	Friday, April 10, 2009
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Sense Pin	Impedance	Codec Signals	Function
SENSE A	39.2K	PORT-A (PIN 39, 41)	Ext. MIC
	20K	PORT-B (PIN 21, 22)	
	10K	PORT-C (PIN 23, 24)	FM tuner
	5.1K	PORT-D (PIN 35, 36)	Headphone out
39.2K	PORT-E (PIN 14, 15)		
20K	PORT-F (PIN 16, 17)		
SENSE B	10K	PORT-H (PIN 37)	Int. MIC
	5.1K	PORT-I (PIN 32, 33)	Headphone out

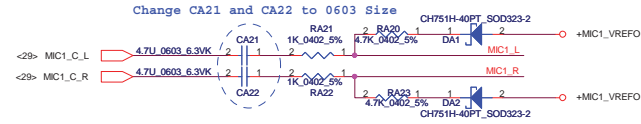
TPA6017 Medium Range Amplifier

Rin = 70Kohm

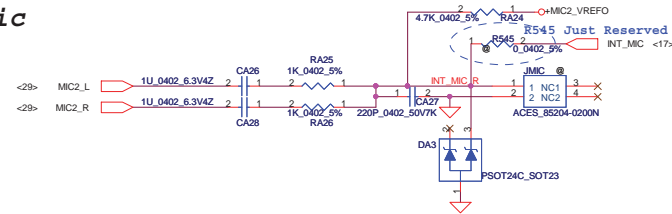


GAIN0	GAIN1	Av (db)	Rin (ohm)
0	0	6	90K
0	1	10	70K
1	0	15.6	45K
1	1	21.6	25K

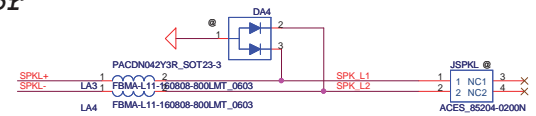
Ext. Mic



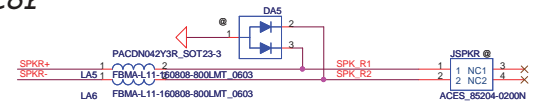
Int. Mic



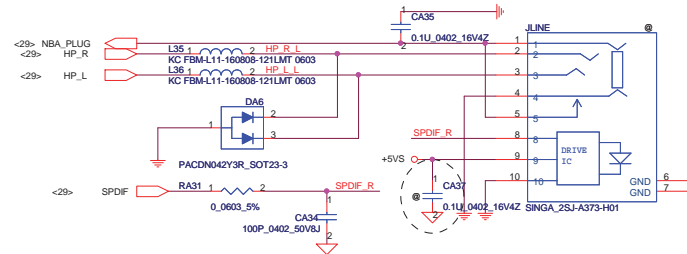
Left Connector



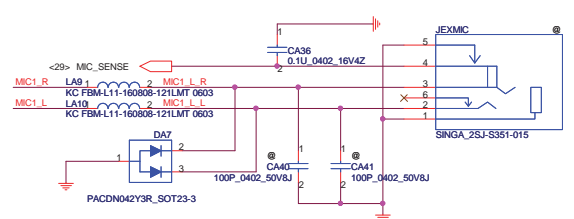
Right Connector

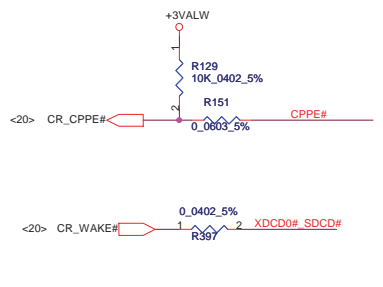
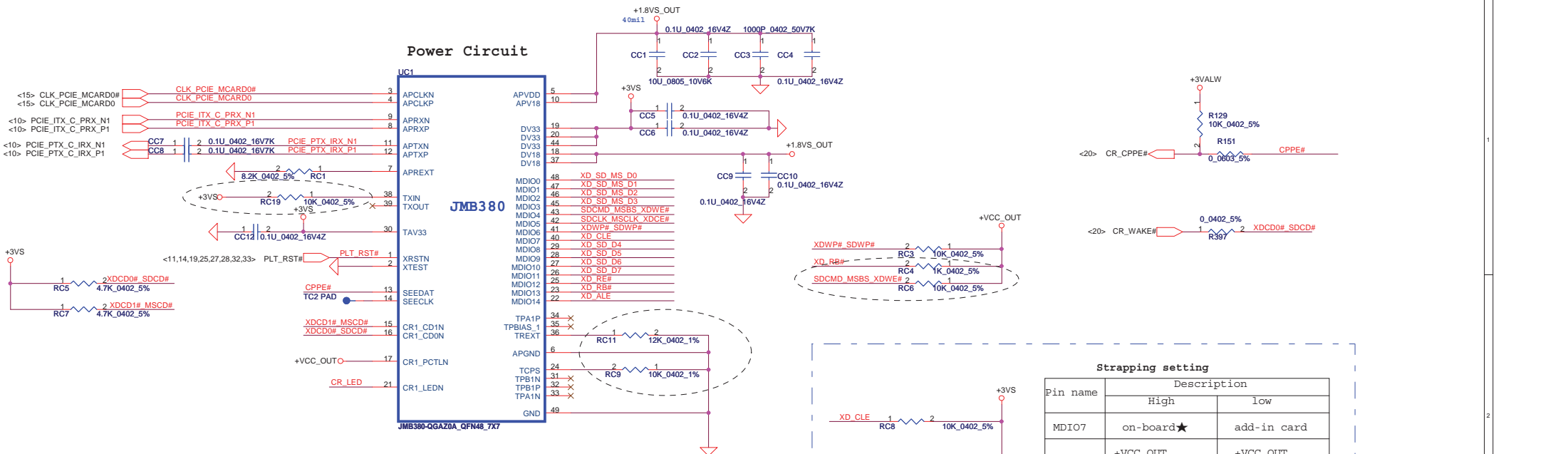


HeadPhone/LINE Out JACK



Ext.MIC/LINE IN JACK

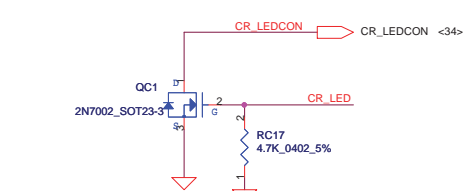




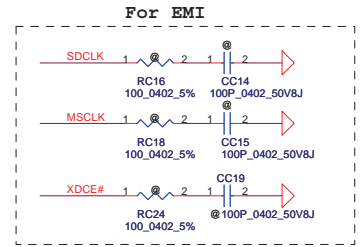
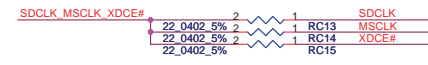
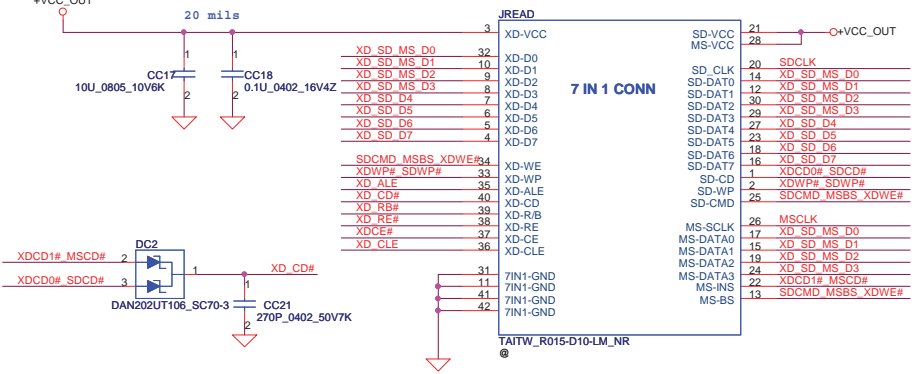
Strapping setting

Pin name	Description	
	High	low
MDIO7	on-board★	add-in card
MDIO12	+VCC_OUT high active	+VCC_OUT low active★
MDIO14	CR_LED high active★	CR_LED low active

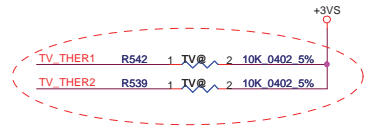
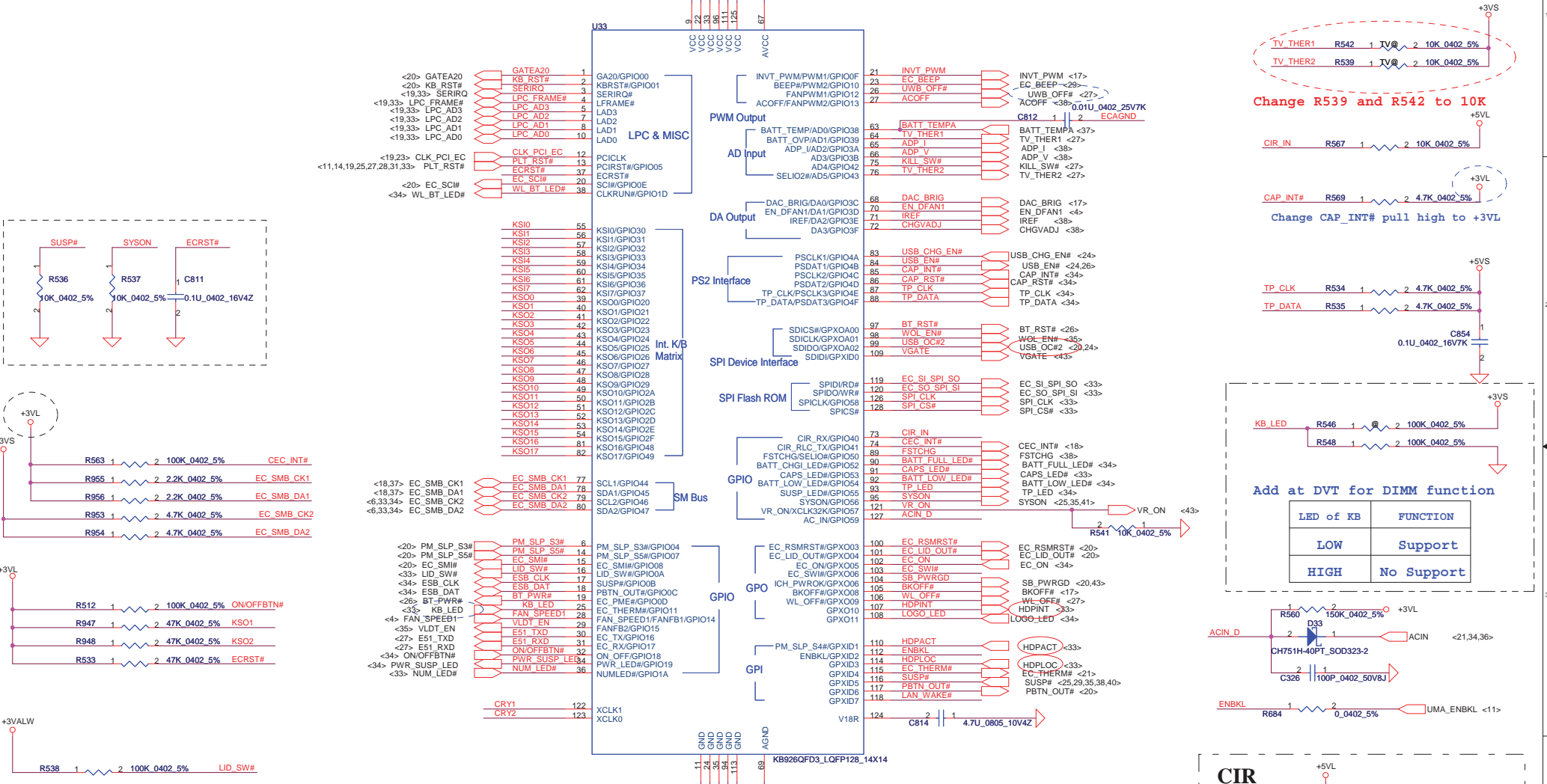
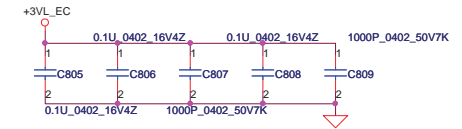
P.S CR1 PCTLN also can out 3V with 250mA for 5IN1 using. (MDIO12 can't be seted after MP IC)



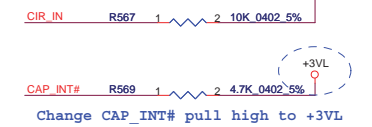
Card Reader Connector



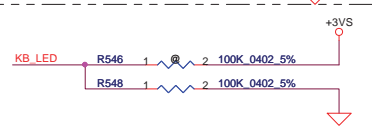
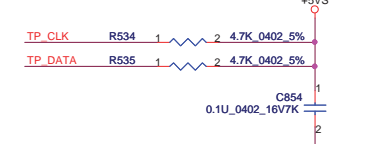
<33,34> KSI[0..7] ← KSI0..7
 <33,34> KSO[0..17] ← KSO0..17



Change R539 and R542 to 10K

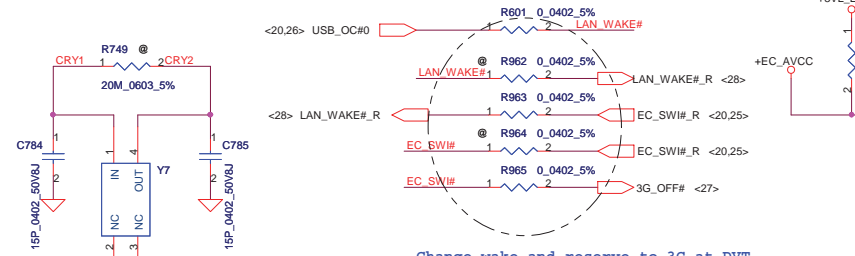
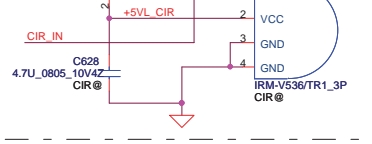
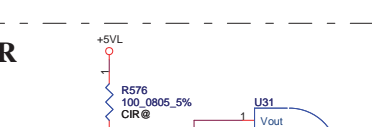
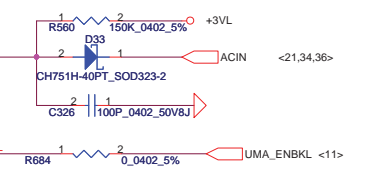


Change CAP_INT# pull high to +3V



Add at DVT for DIMM function

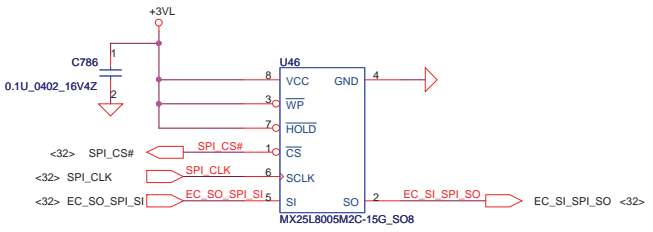
LED of KB	FUNCTION
LOW	Support
HIGH	No Support



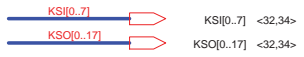
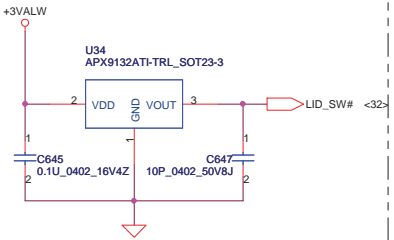
Change wake and reserve to 3G at DVT

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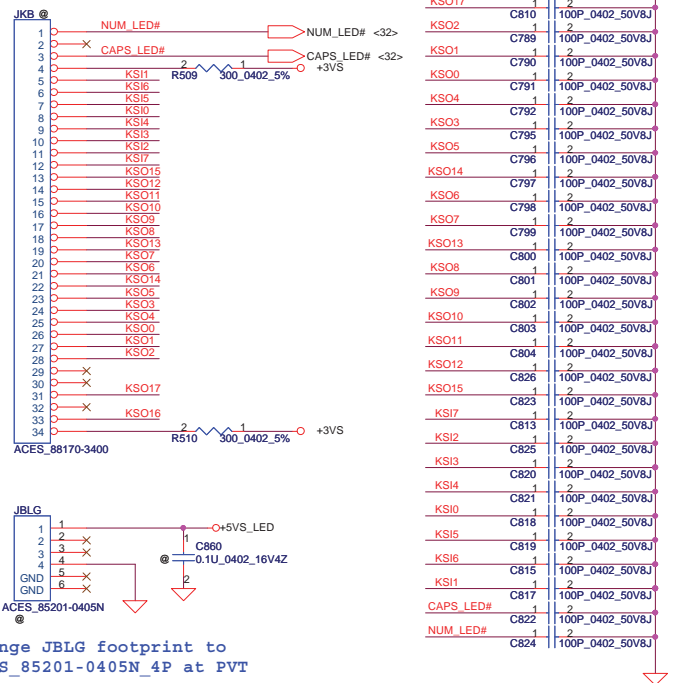
SPI Flash (8Mb*1)



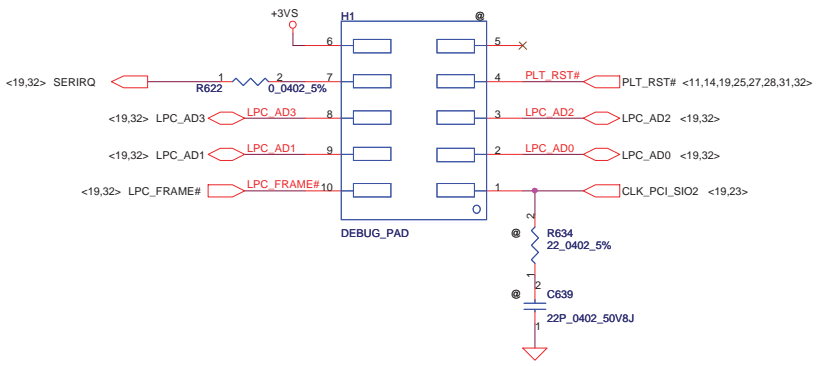
Lid



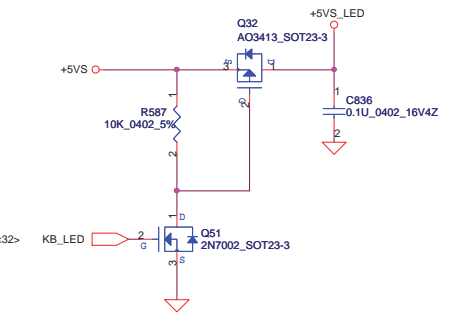
KEYBOARD CONN.



LPC Debug Port (Please place the PAD under DDR DIMM)

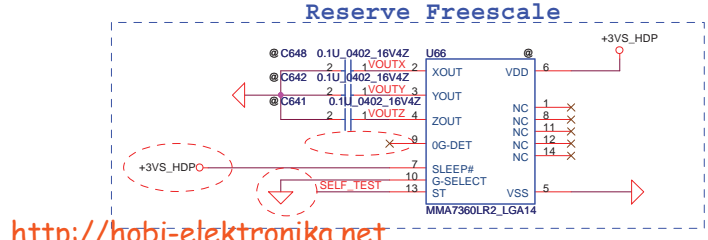
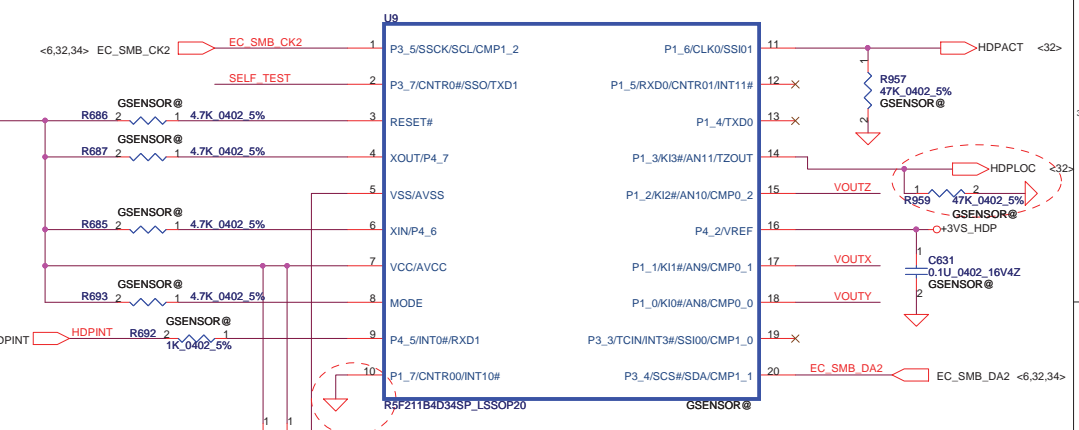
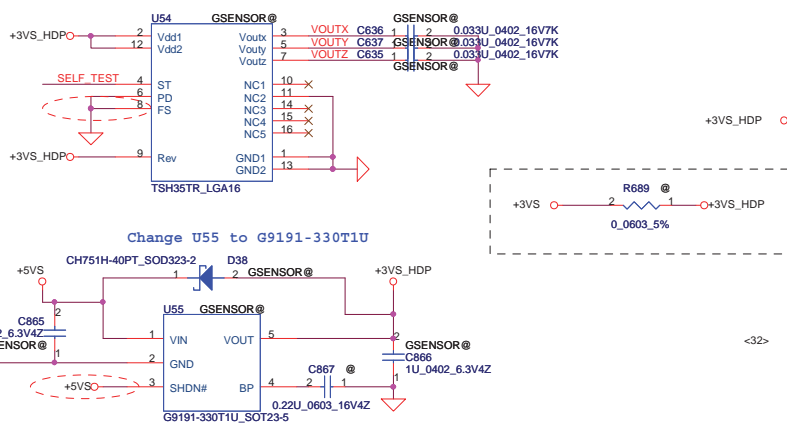


KB LED



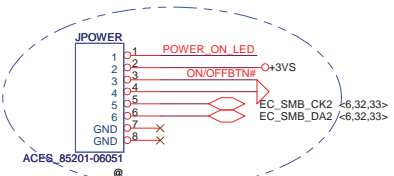
Change JBLG footprint to ACES_85201-0405N_4P at PVT

G-Sensor

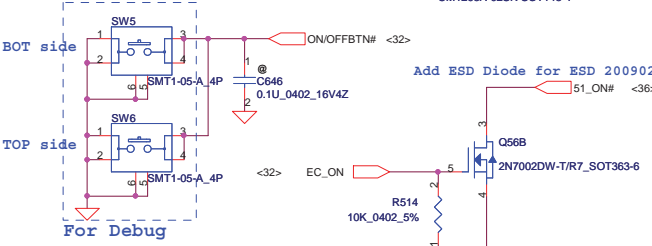
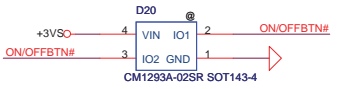


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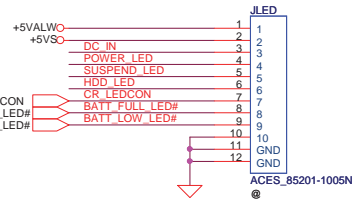
Power Button & PWR/B



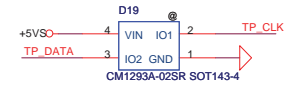
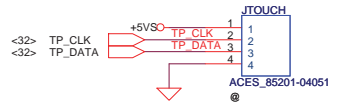
Add Light Sensor at DVT



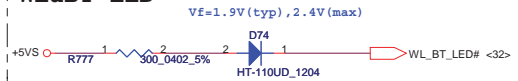
LED/B Connector



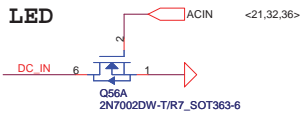
Touch/B Connector



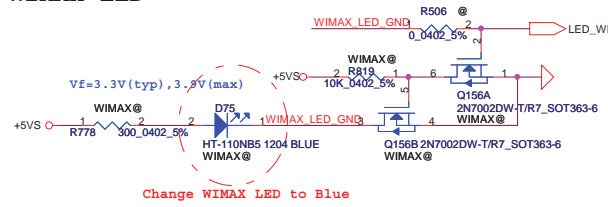
WL&BT LED



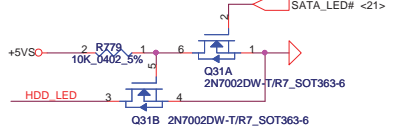
DC-IN LED



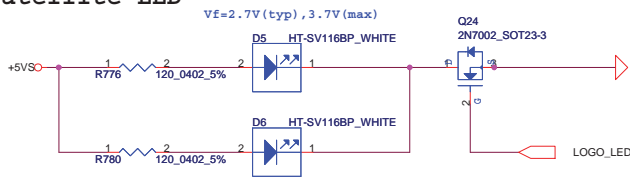
WiMAX LED



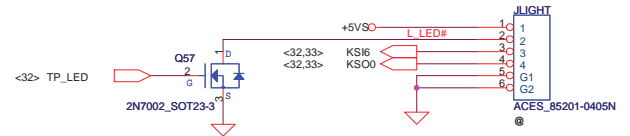
HDD LED



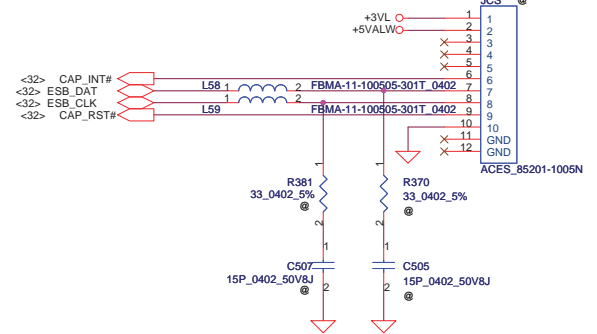
Satellite LED



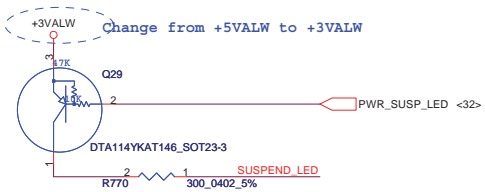
Light Pipe Connector



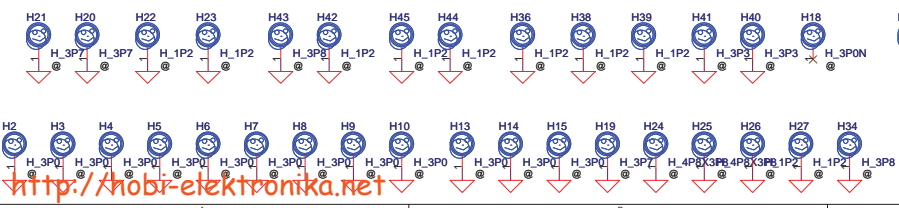
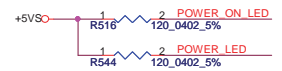
Caps Sensor Connector



SUSPEND LED

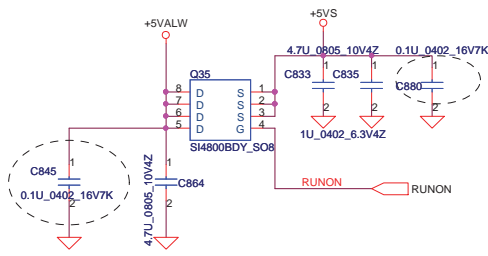


POWER LED

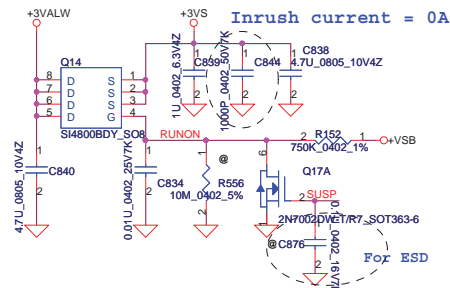


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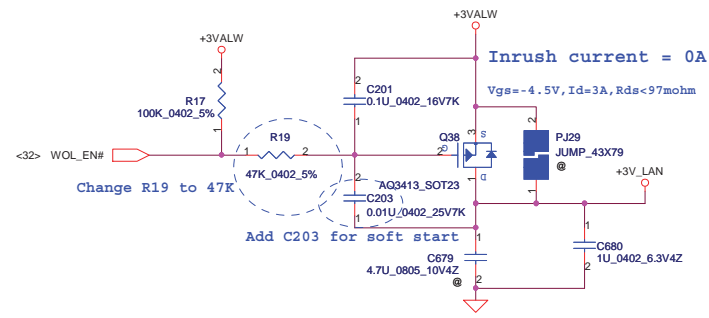
+5VALW TO +5VS



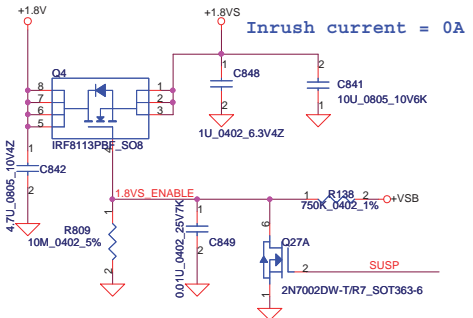
+3VALW TO +3VS



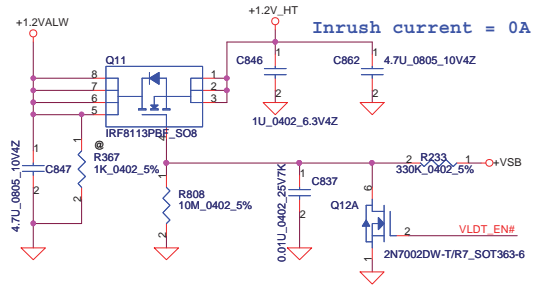
+3VALW TO +3V_LAN



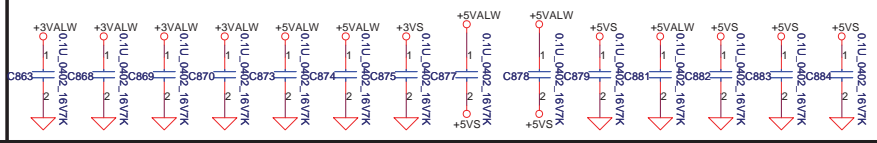
+1.8V TO +1.8VS



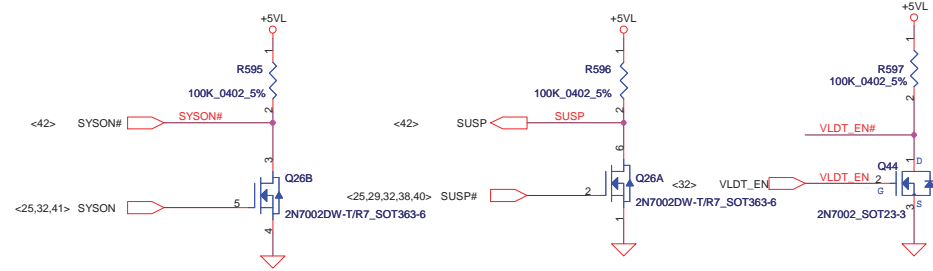
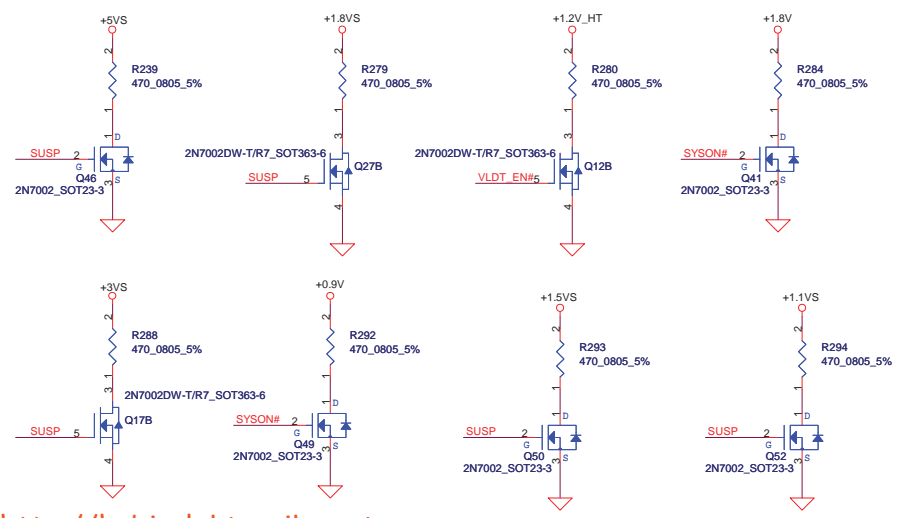
+1.2VALW TO +1.2V_HT



Reserve for ESD



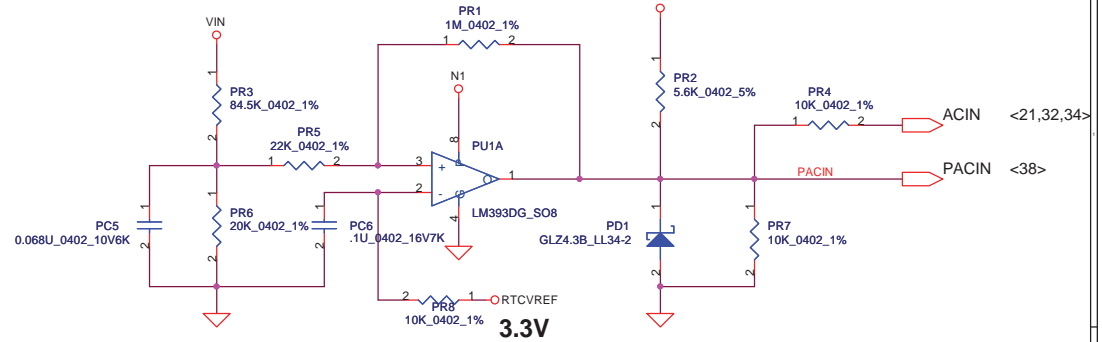
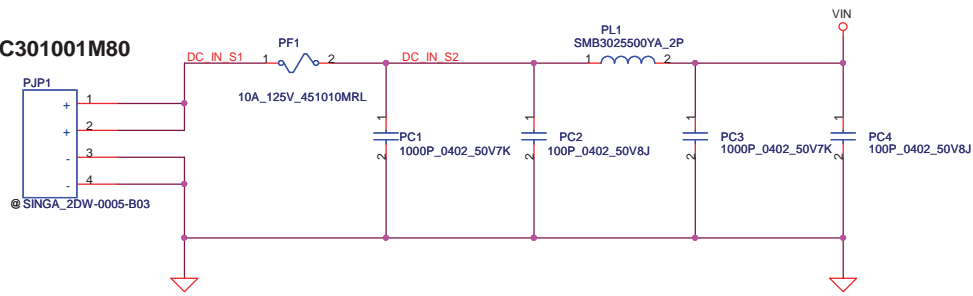
Discharge circuit



<http://hobi-elektronika.net>

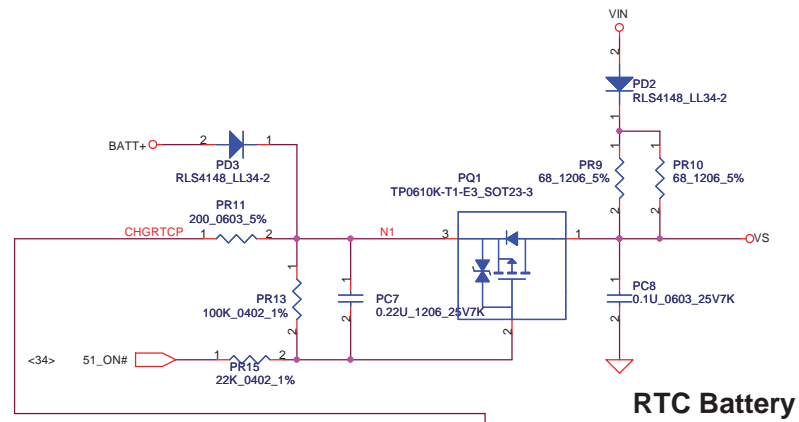
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DC301001M80

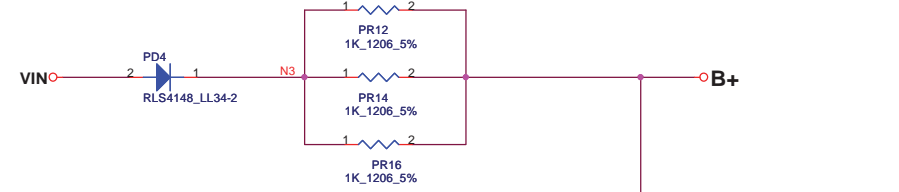
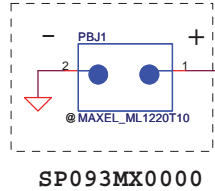


Vin Detector

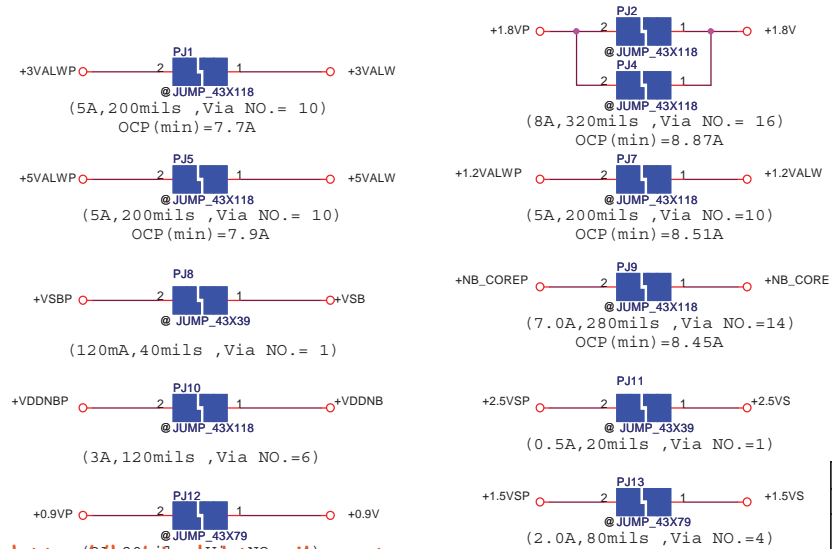
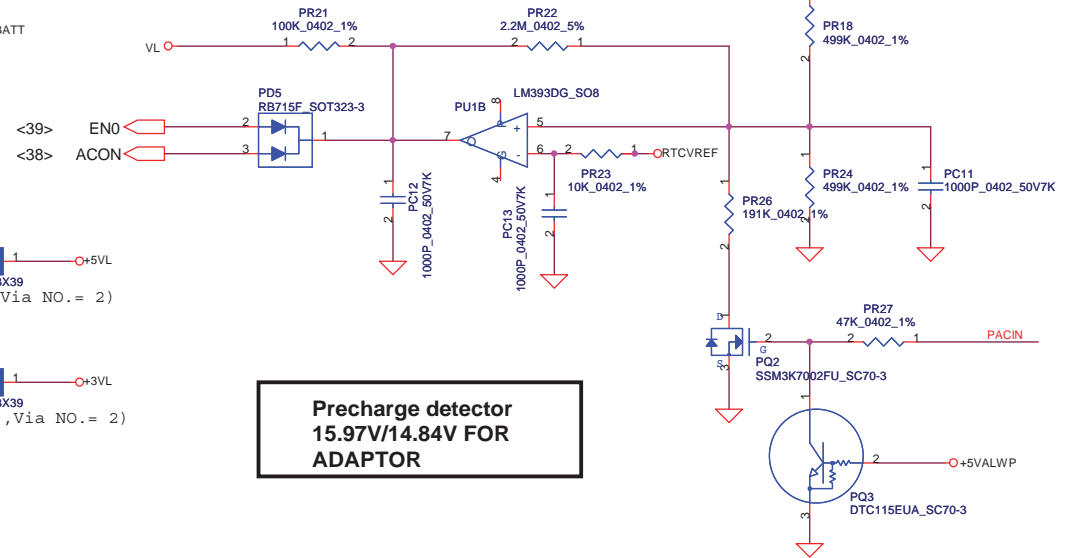
High	18.384	17.901	17.430
Low	17.728	17.257	16.976



RTC Battery

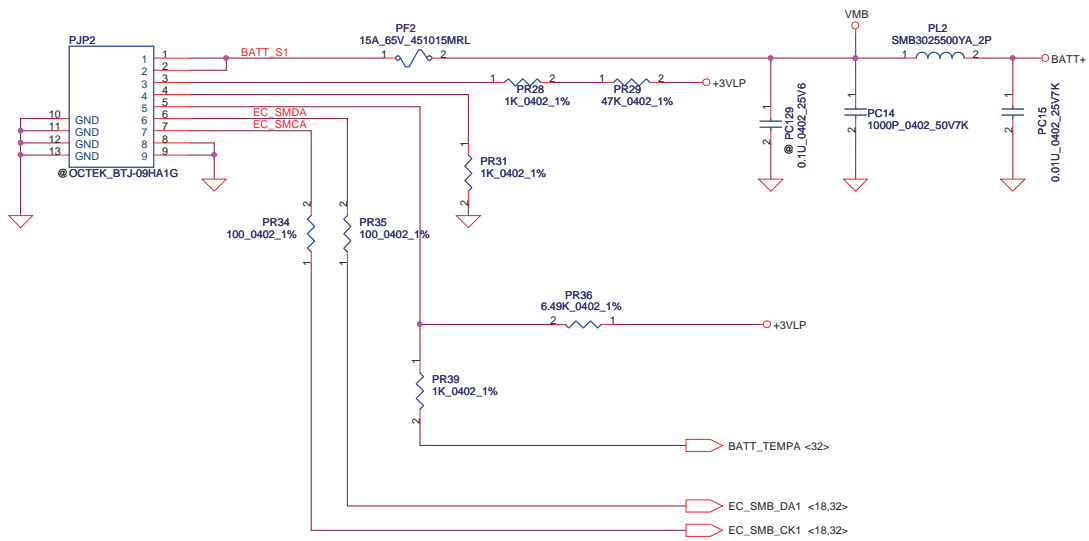


**Precharge detector
15.97V/14.84V FOR
ADAPTOR**

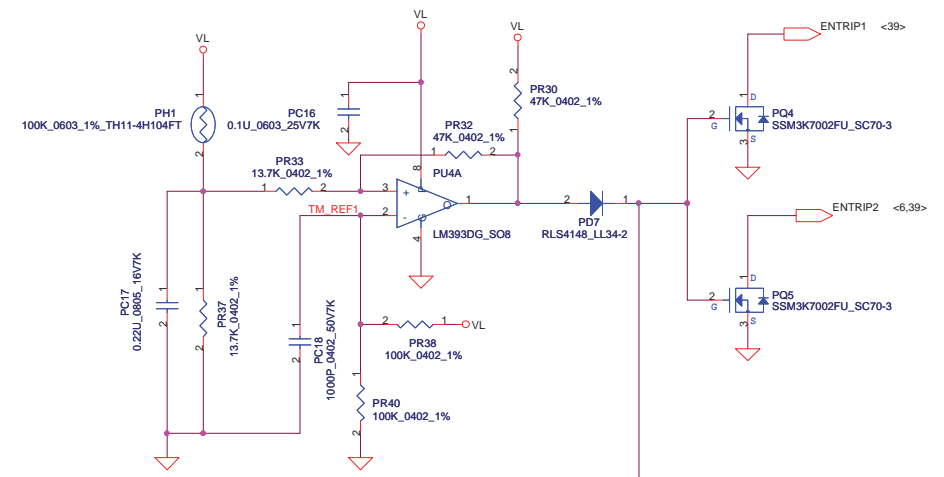


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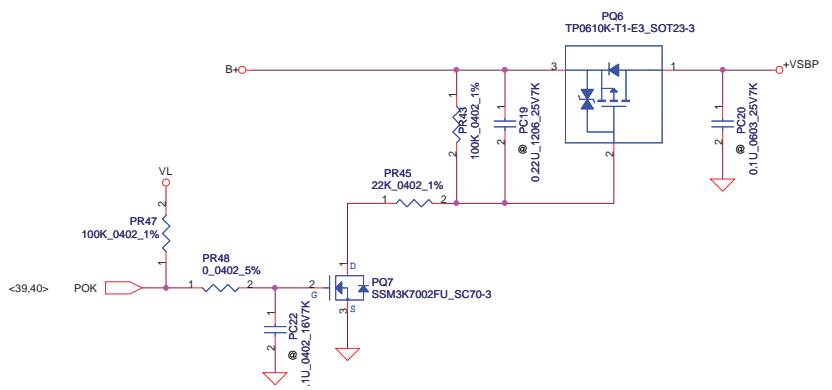
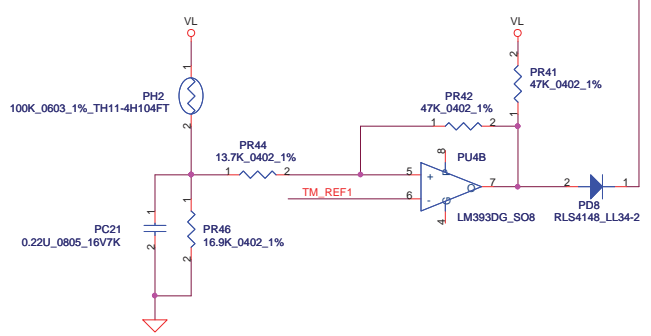
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DCIN/DECTOR			
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PH1 under CPU bottom side :
 CPU thermal protection at 96 degree C
 Recovery at 60 degree C



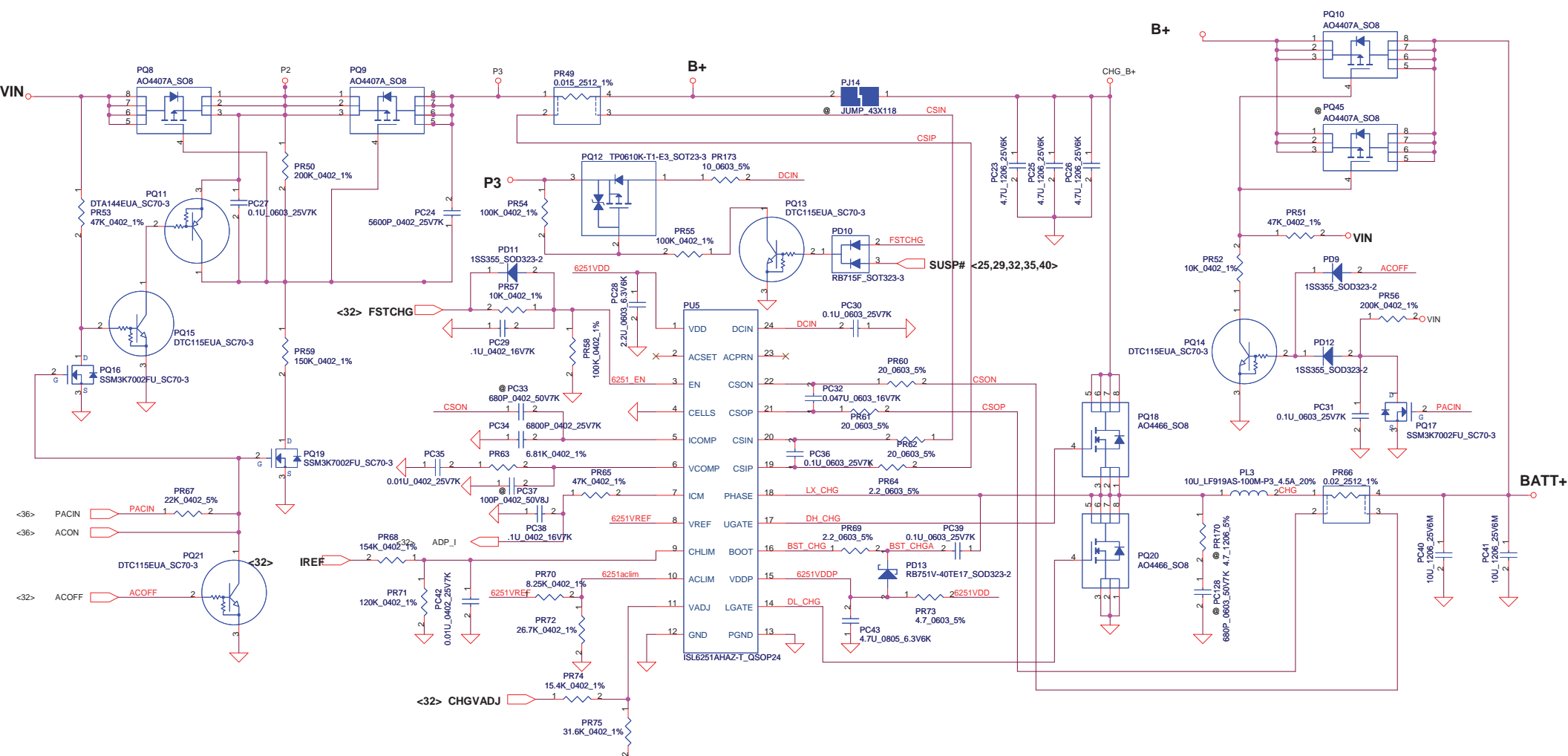
PH2 near main Battery CONN :
 BAT. thermal protection at 90 degree C
 Recovery at 53 degree C



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BATTERY CONN / OTP

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CC=0.25A-3A
 IREF=1.016*Icharge
 IREF=0.254V-3.048V
 VCHLIM need over 95mV

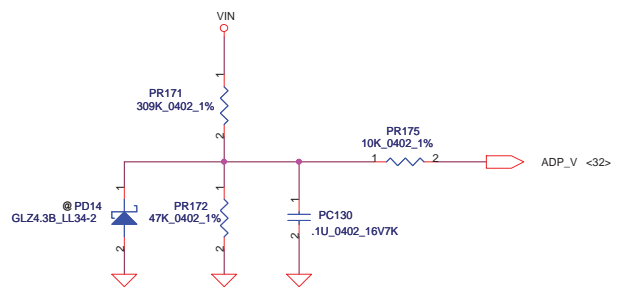
CHGVADJ=(Vcell-4)/0.10627

Vcell	CHGVADJ
4V	0V
4.2V	1.882V
4.35V	3.2935V

Iada=0-3.947A (75W) CP= 92%*Iada; CP=3.65A

CP mode
 $V_{aclim} = 2.39 * (20K // 152K) / (20K // 152K + 24K // 152K) = 1.09986V$
 $I_{input} = (1/0.02) * ((0.05 * V_{aclim}) / 2.39 + 0.05)$
 where $V_{aclim} = 1.09986V$, $I_{input} = 3.65A$

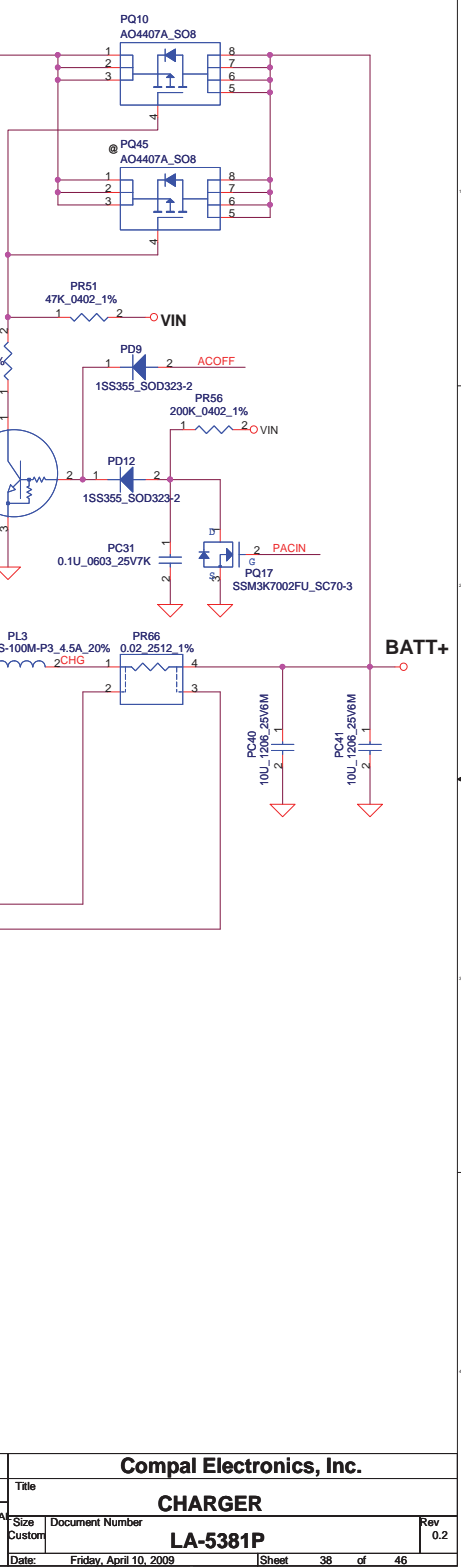
CELLS	VDD	GND	Float
CELL number	4	3	2



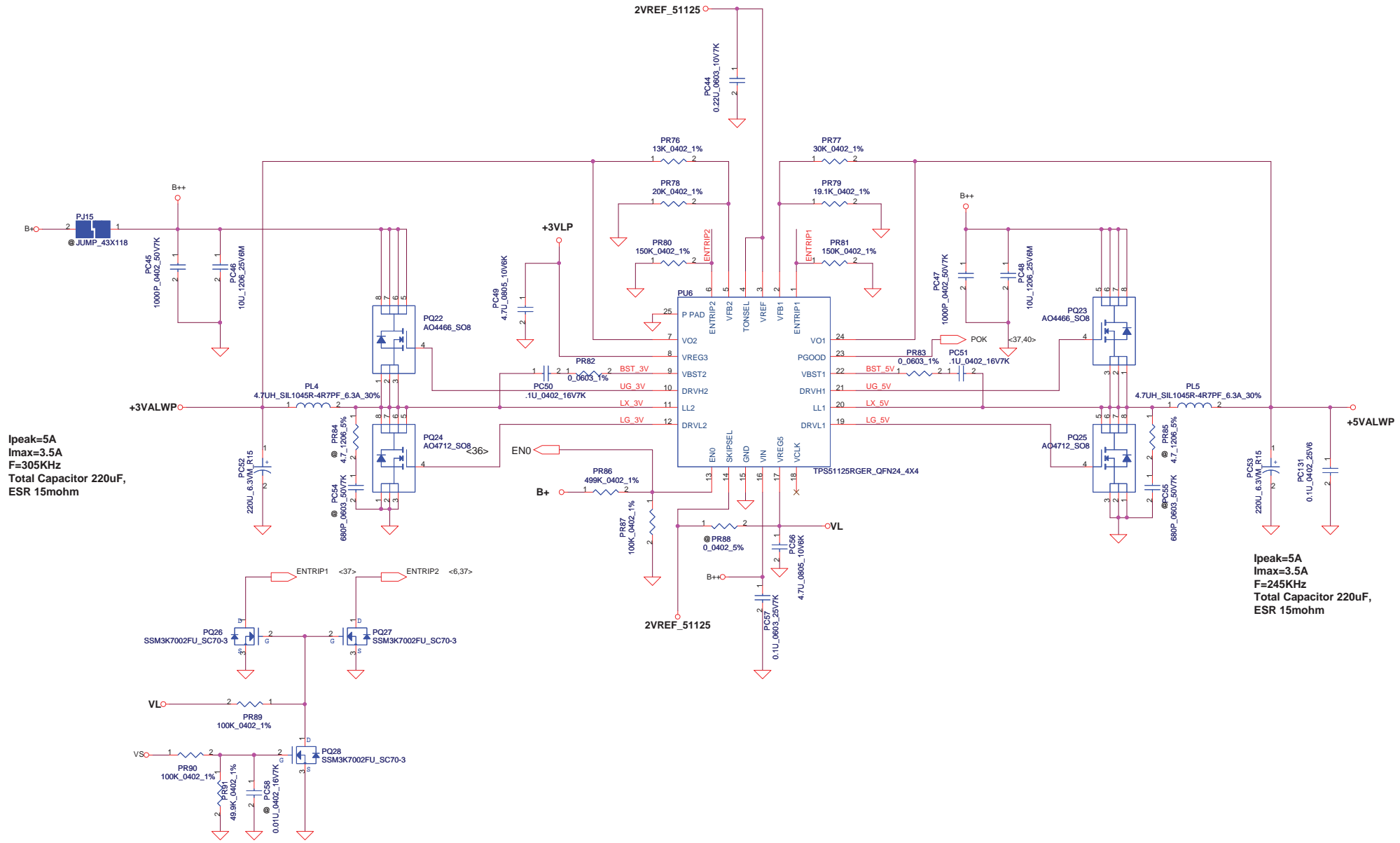
90W Iadapter=0-4.74A PR49=0.015 ohm CP=4.357A PR70=53.6K PR72=20K
 120W Iadapter=0-6.32A PR49=0.015 ohm CP=5.81A PR70=8.25K PR72=26.7K

<http://hobi-elektronika.net>

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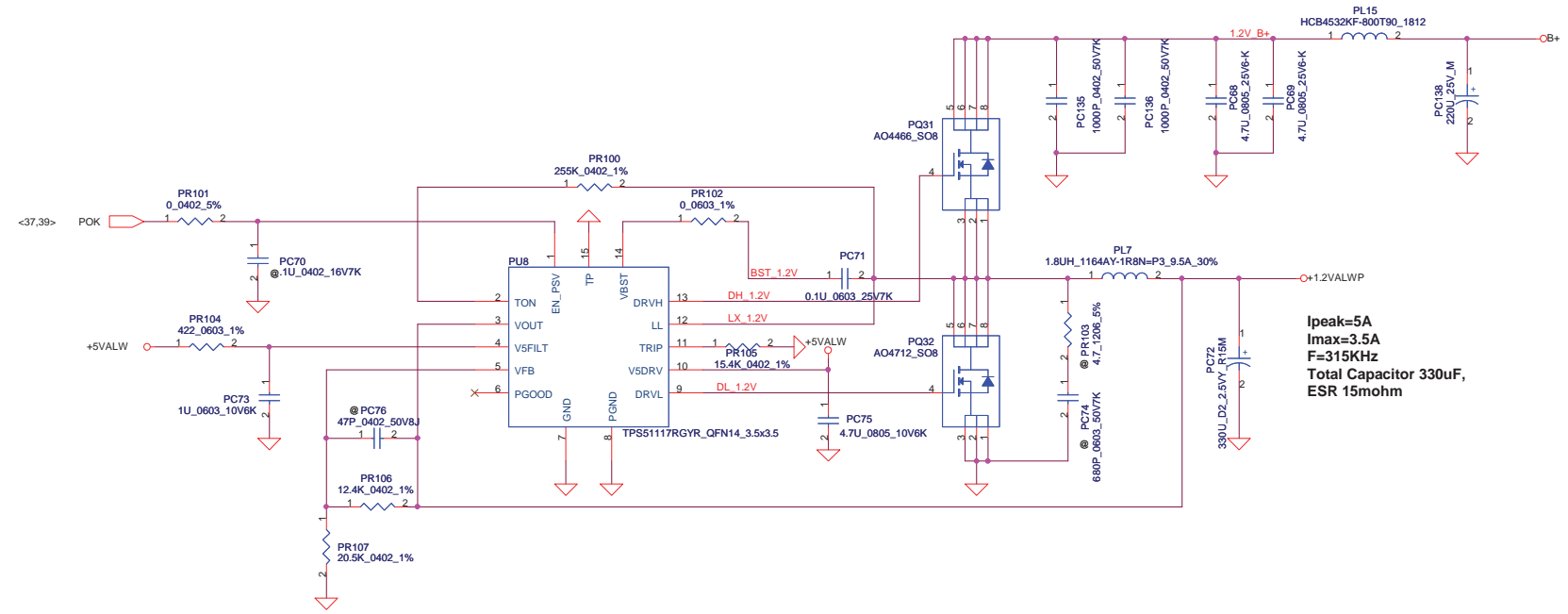
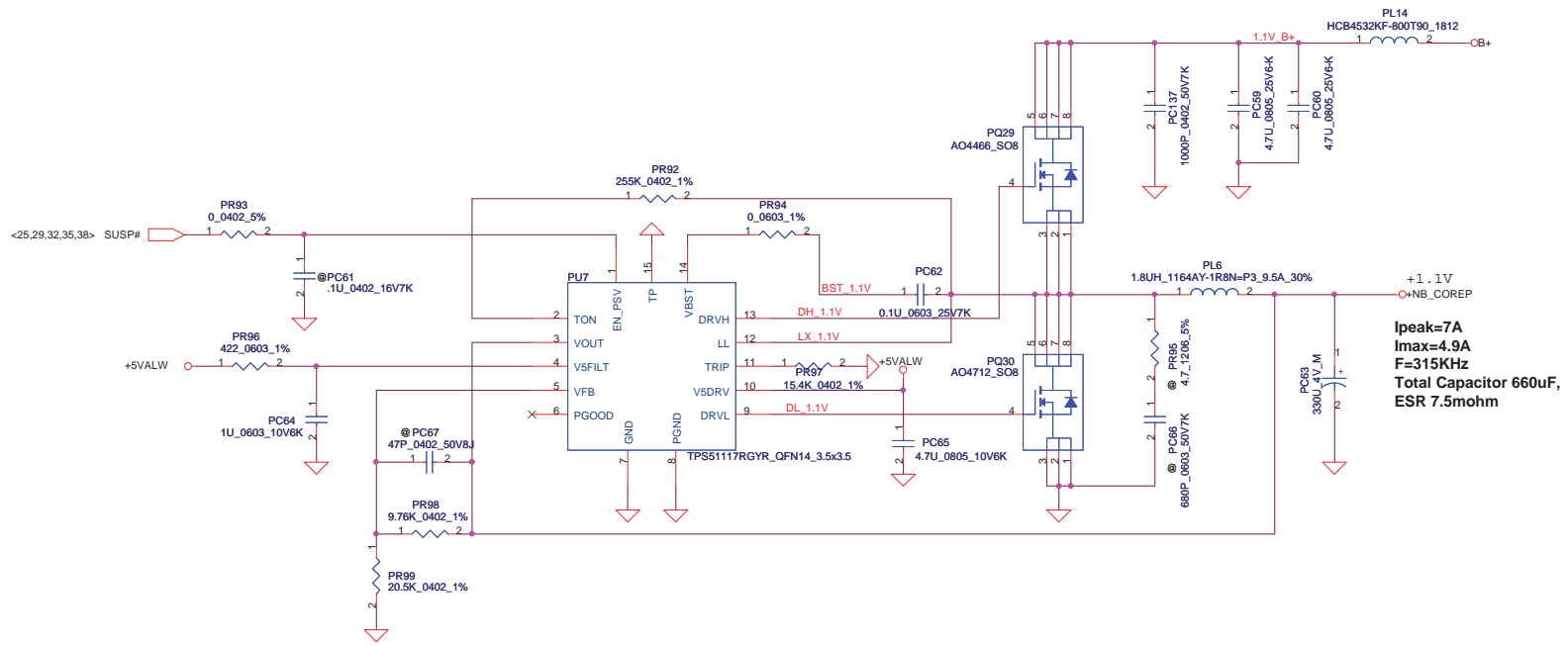
Compal Electronics, Inc.			
CHARGER			
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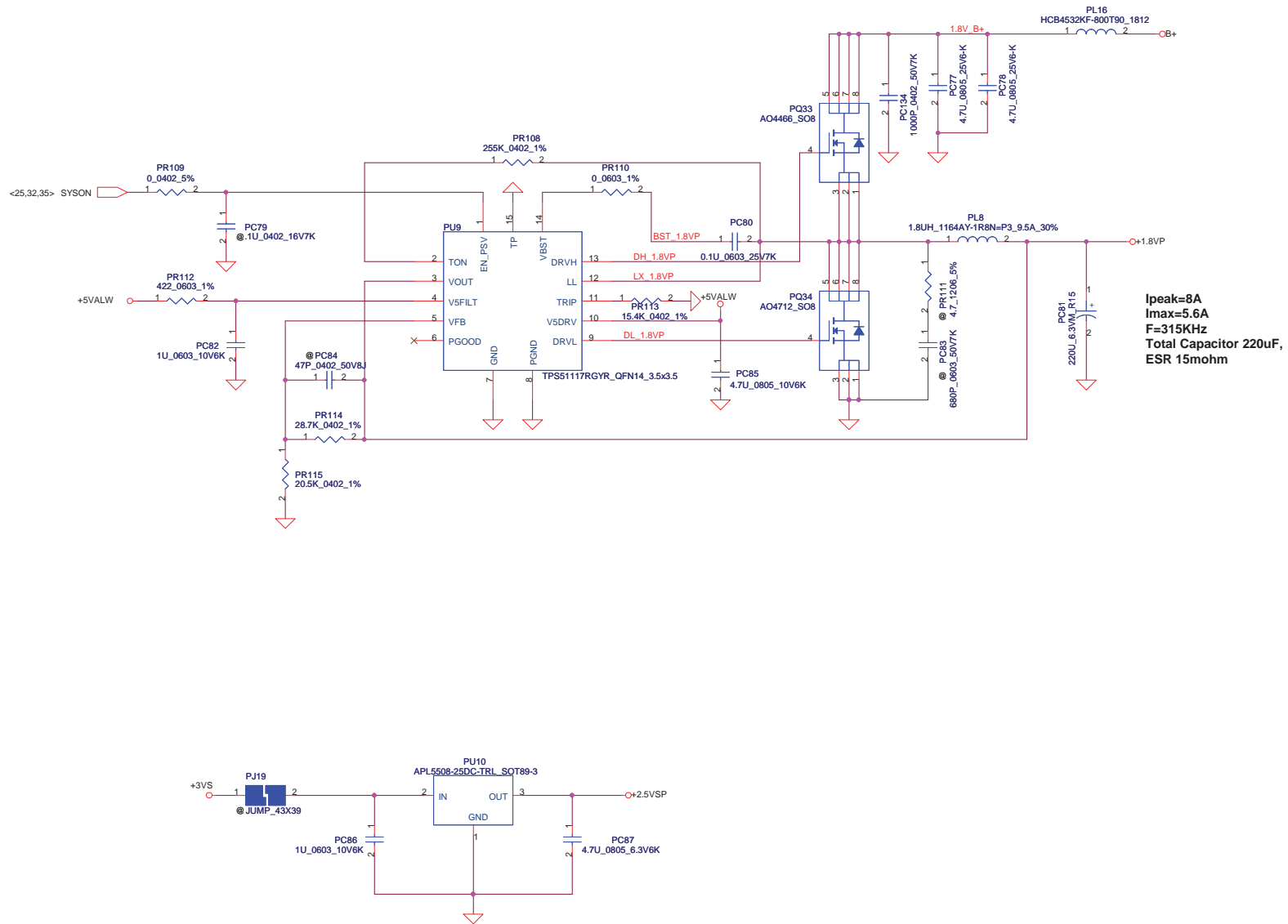
Ipeak=5A
 Imax=3.5A
 F=305KHz
 Total Capacitor 220uF,
 ESR 15mohm

Ipeak=5A
 Imax=3.5A
 F=245KHz
 Total Capacitor 220uF,
 ESR 15mohm

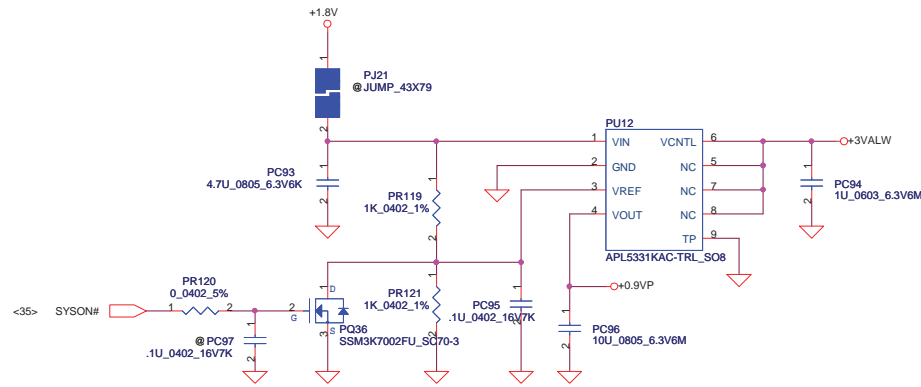
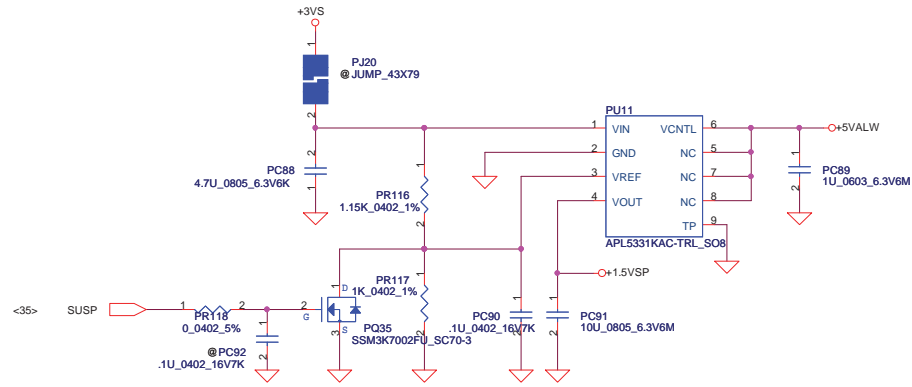
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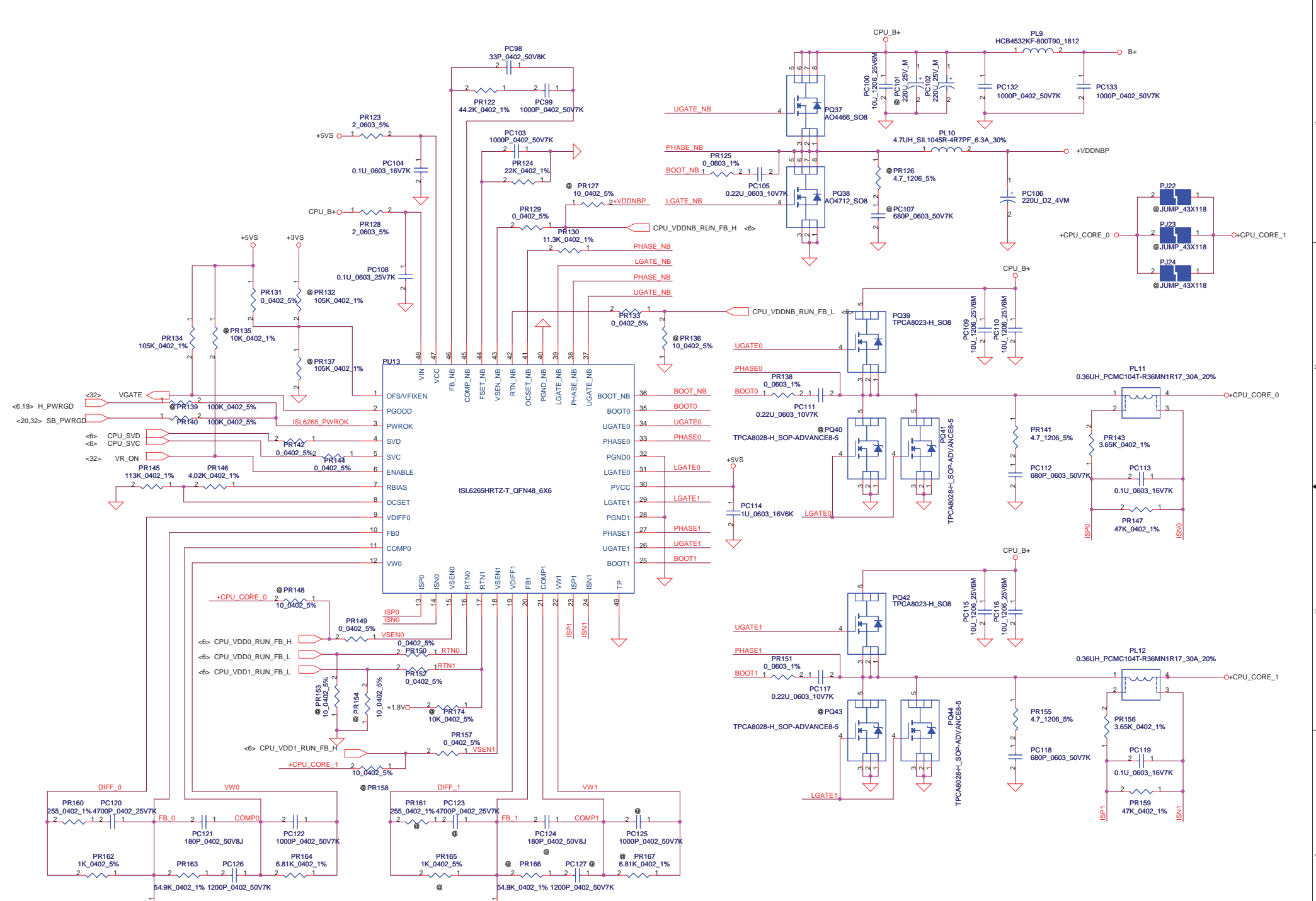
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PCB	<p>ZZZ</p>  <p>PCB LA-5381P REV0</p>
North Bridge	<p>U3</p>  <p>RS880M RS880MR1@</p> <p>U3</p>  <p>RS880MC RS880MCR1@</p>
South Bridge	<p>U15</p>  <p>SB710 SB710R1@</p>
LAN Controller	<p>UL1</p>  <p>8103EL 8103EL@</p>
LAN Transformer	<p>UL3</p>  <p>10/100M transformer 8103EL@</p>

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HW4 Product Improvement Record (P.I.R.)

NSKAE LA-5381P SCHEMATIC CHANGE LIST
 REVISION CHANGE: 0.1 TO 0.2
 GERBER-OUT DATE: 2009/04/06

NO	DATE	PAGE	MODIFICATION LIST	PURPOSE
1	3/10	17	Change R156 to 10K pull down	Special LCD issue
2	3/10	30	Change RA16 to 1% tolerance	Codec requirement
3	3/10	33	Add R962-R965	Reserve GPIO to EC
4	3/13	22	Add R193-R196	Strap pin for SW
5	3/23	16	Add R540	Common Design
6	3/24	30	Add CA49, CA50	GPS issue
7	3/24	30	Add CA51-CA54	Common design
8	3/24	27	Add R722 and C754	Common design
9	3/25	27	Add R423	Common design
10	3/25	28	Add RM7 for Wimax module	Wimax issue
11	3/25	28	Add R822	Customer Request
12	4/9	31	Change UC1 from JMB385 to JMB380	For ME height limit
13	4/9	35	Add C863 to C884	For EMI request
14	4/9	18	Delete Q161 and add D53	For customer request
15	4/9	16	Delete Q162 and add D21	For customer request

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Version Change List (P. I. R. List) for Power Circuit

Page#	Title	Date	Request Owner	Issue Description	Solution Description
44	EVT	2009/02/25	POWER		NSKAE for Tigirs (UMA)
39	EVT	2009/03/16	POWER		For CHGVADJ (memo)
41	EVT	2008/12/30	HW		meet AMD RS780 SPEC (memo)
41	EVT	2009/02/10	POWER		Noise (memo)
41-42	DVT	2009/03/31	POWER		Noise
40	DVT	2009/03/31	HW		For HDMI
41	DVT	2009/03/31	POWER		Noise
41-42	DVT	2009/03/31	POWER		Noise
41-42	DVT	2009/03/31	POWER		For EMI
39	DVT	2009/03/31	POWER		For ADP_I
40	DVT	2009/03/31	POWER		For common circuit
39	DVT	2009/03/31	POWER		For 12 Cell charge 3.6A
41	DVT	2009/03/31	HW		Change to 12.1K and 19.6K
44	PVT	2009/03/31	POWER	No issue	Change to common parts

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